ELECTRONICS WORKSHOP PROJECT

CLASS-D POWER AMPLIFIER

PROJECT MENTOR

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PROJECT TEAM

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OBJECTIVE OF PROJECT

- To design class-D power amplifier
- In Classes A, B and AB, the problem is lack of efficiency. Some power is wasted, and we would prefer that it could be sensibly employed in driving the loudspeakers to ever-higher sound pressure levels — or, at least, not converted to heat.

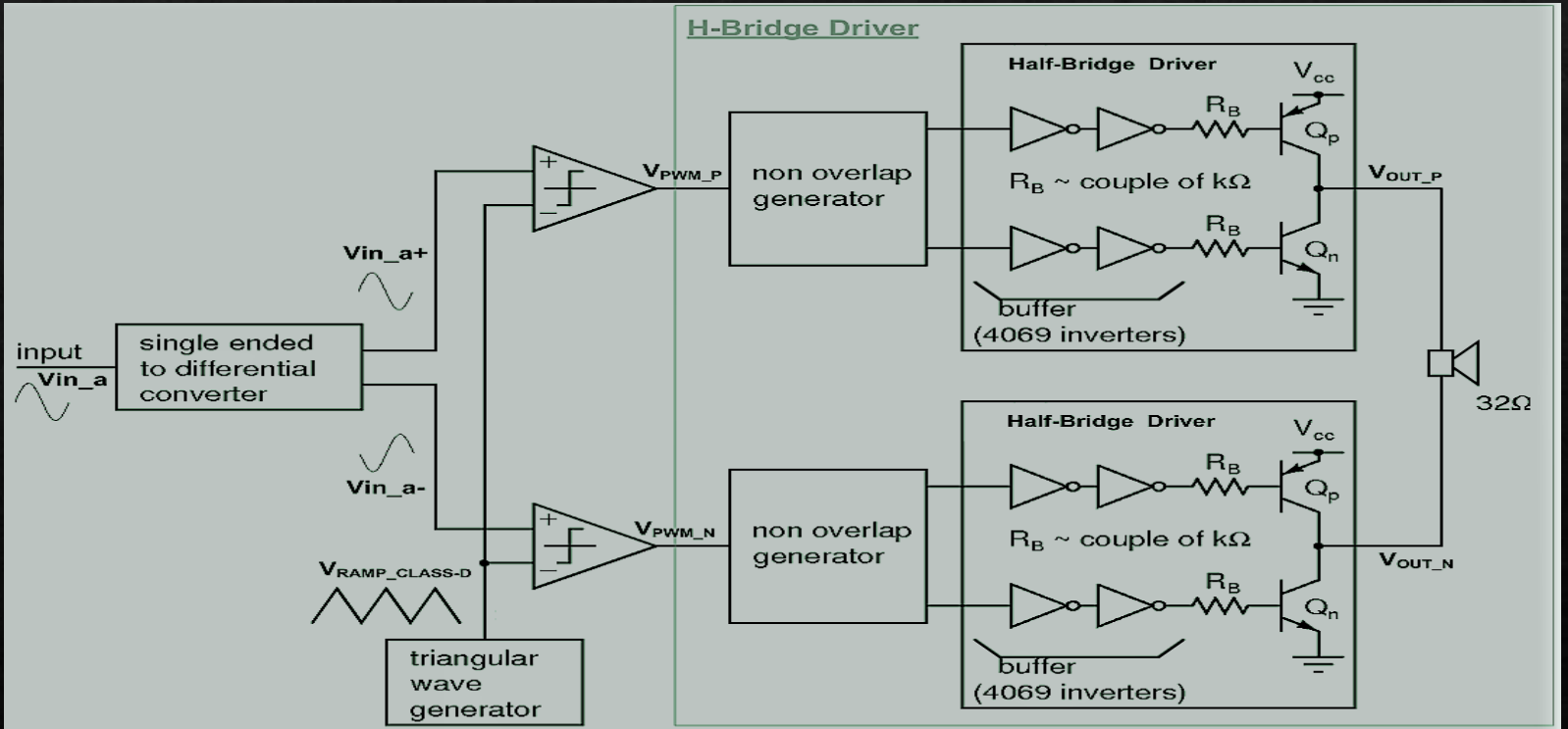


Figure 3-7 Circuit diagram of the complete class-d amplifier

WORKING

- The Class D amplifier converts the input analog signal into a pulse width modulated (PWM) waveform.
- The PWM waveform drives the push-pull FET output stage fully on or off for each pulse.
- The analog signal is initially passed through a single-ended to differential converter, which enables us to obtain a inverted version which when converted to PWM drive the FET.
- The PWM signal obtained previously is amplified by the switching MOSFETs.
- The H-bridge has two switching circuits that supply pulses of opposite polarity to the filter, which comprises two inductors, two capacitors, and the speaker. Each half-bridge contains two output transistors—a high-side transistor (MH) connected to the positive power supply, and a low-side transistor (ML) connected to the negative supply.
- For a given VDD and VSS, the differential nature of the bridge means that it can deliver twice the output signal and four times the output power of single-ended implementations.
- In the switching, for an instance, both the NMOS and PMOS are switched on and short circuit power dissipation takes place. To avoid this, delay elements and dead time control are used.
- A second-order Butterworth L-C filter is used as a low pass filter to obtain the amplified analog signal. It removes unnecessary frequencies and gives out the required signal.

WORKING

BLOCK DIAGRAM

TRIANGULAR WAVE GENERATOR

SINGLE ENDED TO DIFFERENTIAL CONVERTER

PWM GENERATION BY COMPARING TRIANGULARE WAVE AND DIFFERENTIAL OUTPUTS

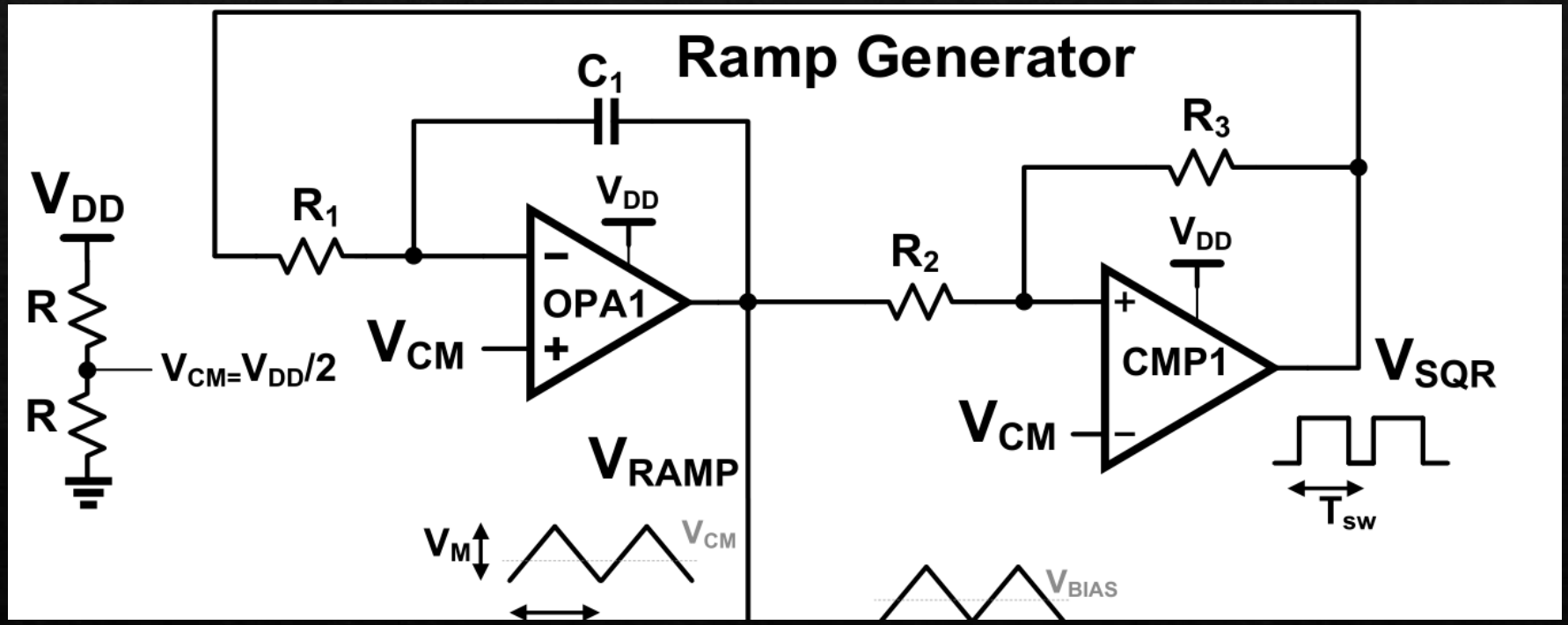
DEAD TIME CONTROL (NON OVERLAP GENERATOR)

SWITCHING STAGE (GATE DRIVER AND POWER MOSFETS)

LOW PASS LC FILTER (BUTTER WORTH)

TRIANGULAR WAVE GENERATOR

- Ramp or triangle wave generator is actually an oscillator which is designed using opamp -RC integrator and Schmitt trigger.
- PWM is generated by comparing the ramp signal (V RAMP) with control signal (V CTRL). Common mode voltage of ramp signal should be around V DD /2 hence might require to decouple the dc voltage and set common mode at V BIAS (around V DD /2).
- The peak-peak amplitude of the ramp is defined by the equation: $VM = 2\left(\frac{R2}{R3}\right)V\text{CM}$
- The oscillation frequency of the ramp is given by equation: $F = R3/(4 * R1 * R2 * C1)$



SINGLE ENDED TO DIFFERENTIAL CONVERTER

- Single ended-to-differential converter can also be designed using op-amp based inverting amplifier

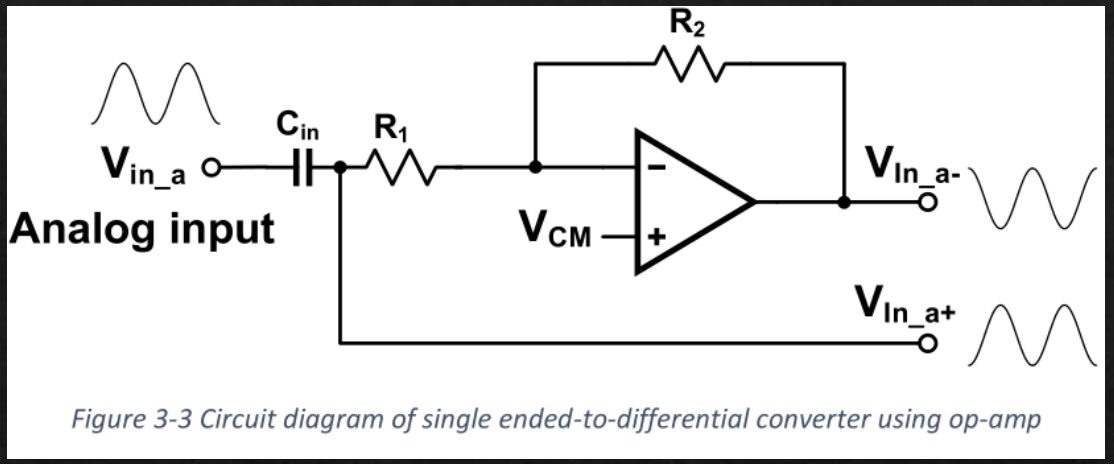
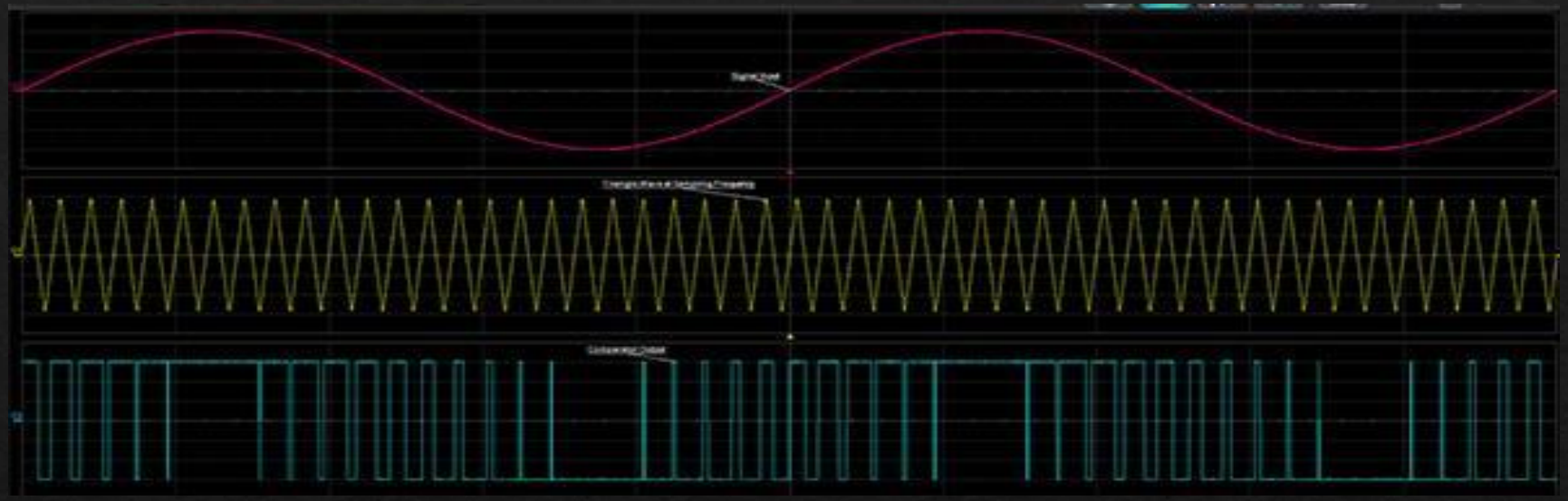


Figure 3-3 Circuit diagram of single ended-to-differential converter using op-amp

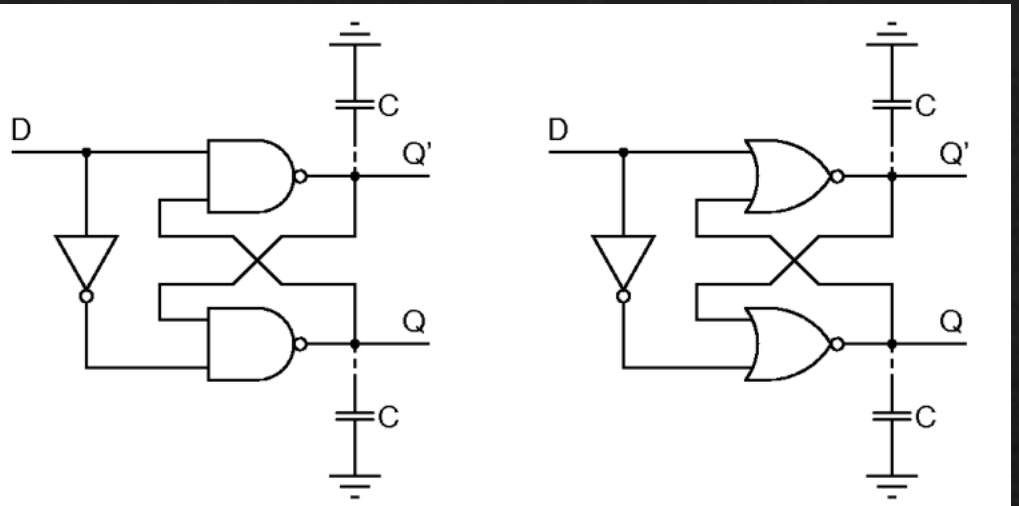
PWM GENERATION USING RAMP AND DIFFERENTIAL OUTPUT

- The ramp here generated is 100 KHz. We use this ramp to sample the differential output. Here the sampling frequency is so high so as to retain the information of signal.
- Whenever the input signal is more positive than the reference triangle wave, a positive pulse is produced that lasts as long as the input signal is above the threshold set by the triangle wave. With a perfect triangle wave, it is easy to see that the pulse width is linearly proportional to the input amplitude.
- Conversely, when the input signal is below the time-varying threshold set by the triangle wave, the output of the comparator is negative.
- The output of the comparator is thus a square wave whose duty cycle corresponds to the amplitude of the input-signal voltage. The frequency of the square wave is referred to as the carrier frequency. It is easy to see that the average value of the square wave is an accurate representation of the input signal.



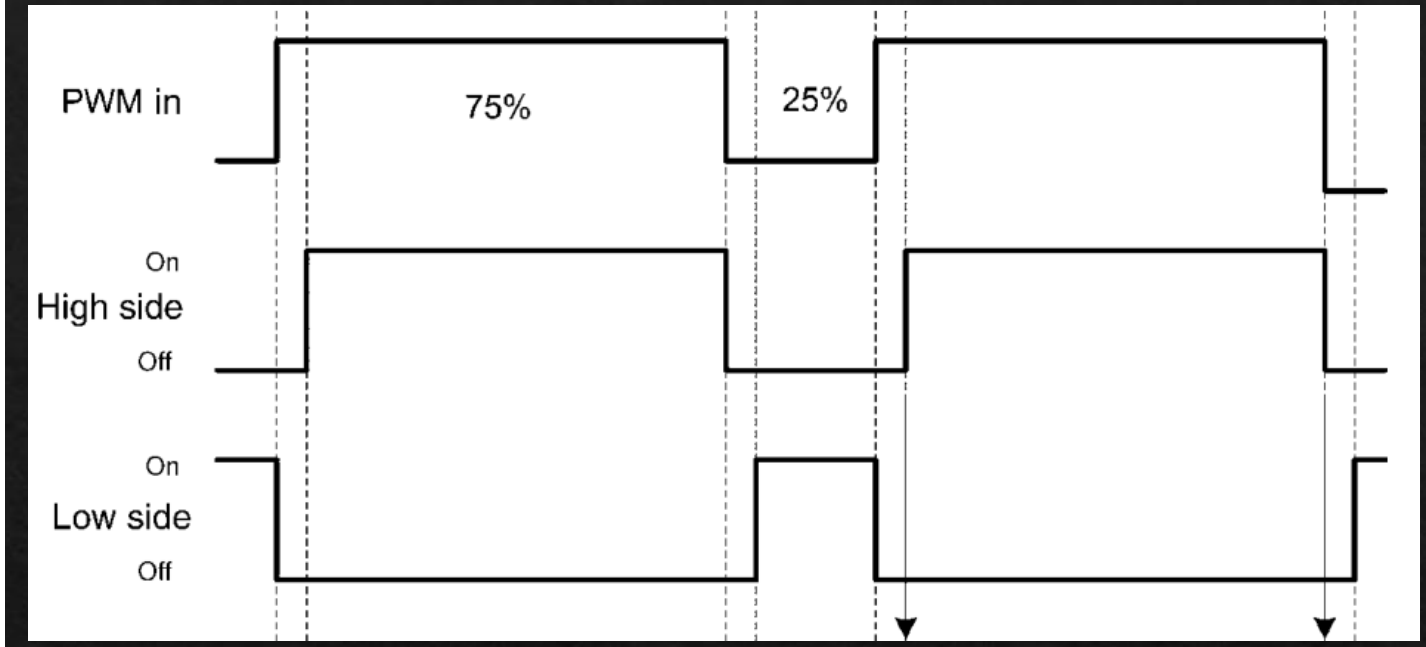
DEAD TIME CONTROL

- When switches are connected from both the positive and negative rails to a single output node, there is always the possibility that both switches will briefly be on at the same time.
- This will cause shoot-through current to flow directly from the positive supply to the negative supply. At minimum, this will result in wasted power (short circuit power dissipation) . In some cases it will result in the destruction of the output stage. For this reason there is a very small dead zone incorporated into the MOSFET drive circuit. This ensures that there is always a very small time when both devices are turned off.



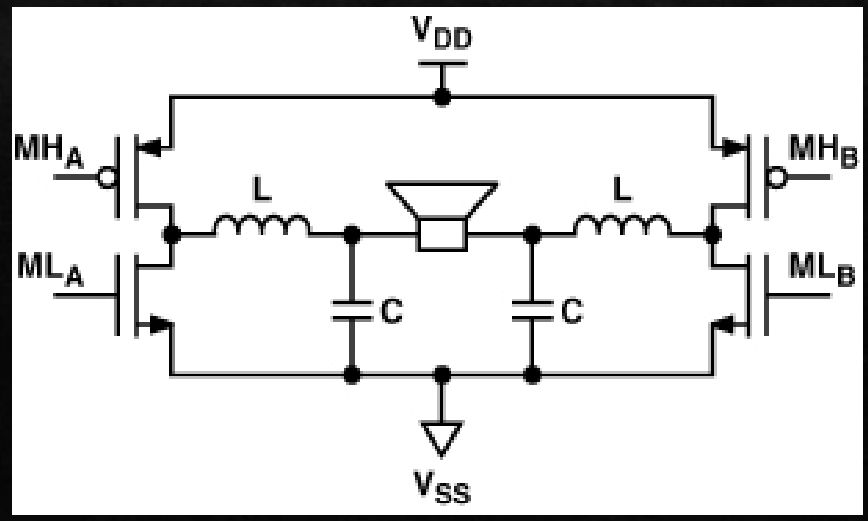
Non overlap generator-an additional inversion is necessary on one of the inputs to drive the p and n switches

Figure 3-5 Non-overlap clock generator



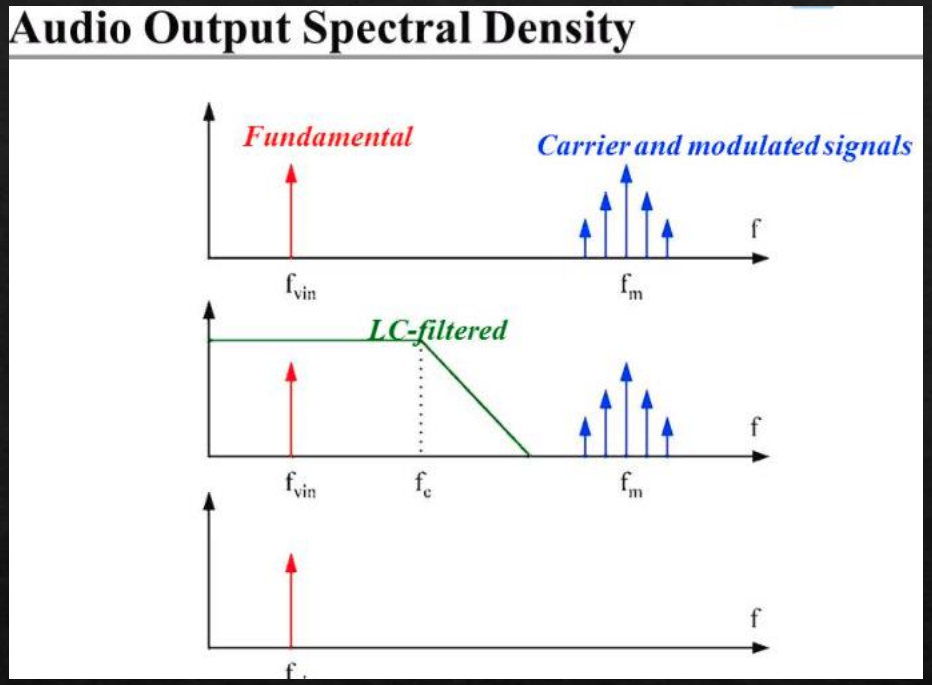
GATE DRIVER AND SWITCHING STAGE

- The H-bridge has two switching circuits that supply pulses of opposite polarity to the filter, which comprises two inductors, two capacitors, and the speaker. Each half-bridge contains two output transistors—a high-side transistor (MH) connected to the positive power supply, and a low-side transistor (ML) connected to the negative supply.



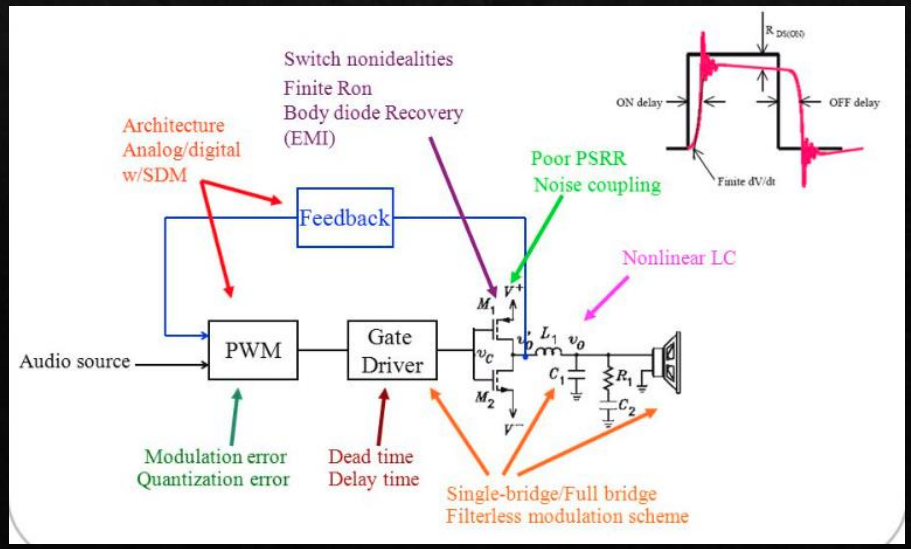
2ND ORDER BUTTERWORTH LC FILTER

- It is used to filter the high frequency triangular wave and retain original sine wave.
- This is done using LC filter.



CHALLENGES FACED

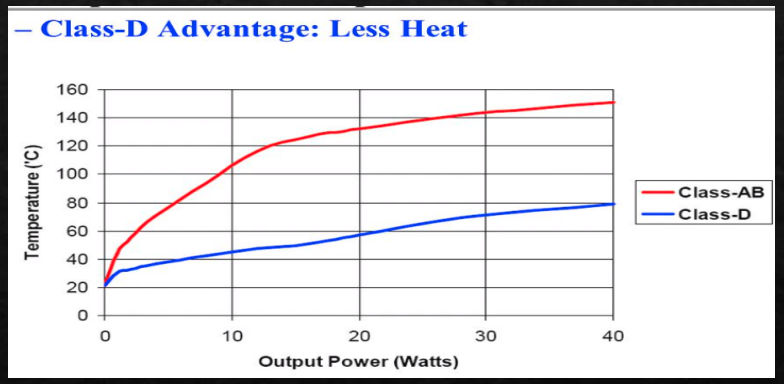
- The PWM produced has ON delay and OFF delay and is affected by Gibbs phenomenon.
- Poor PSRR Noise coupling in switching stage.
- Dead time control and delay time in gate driver.
- Non linearities in LC filter.



ADVANTAGES OF CLASS-D POWER AMPLIFIER

1.High Efficiency

The PWM signal generated drives the push-pull FET output stage of the amplifier. When the FET is on, the current through it is high. But, the voltage across it is low. So the power is very low(~0). Similarly, when the FET is off, the current through it is almost zero. Hence the power is again zero. The only power dissipated is during switching (Dynamic Power). So it has a higher efficiency than the previous models. (~ 80-90%)



2.Low Power Dissipation-Smaller Size

In Class-D amplifiers,

Total power dissipated= P(switching)+P(gate-drivers)+P(conduction)

So, the heat dissipation is low and hence smaller heat sinks will suffice. Also, this means that almost all the power drawn is converted efficiently.

THANK YOU