Characterisation of 6T-SRAM

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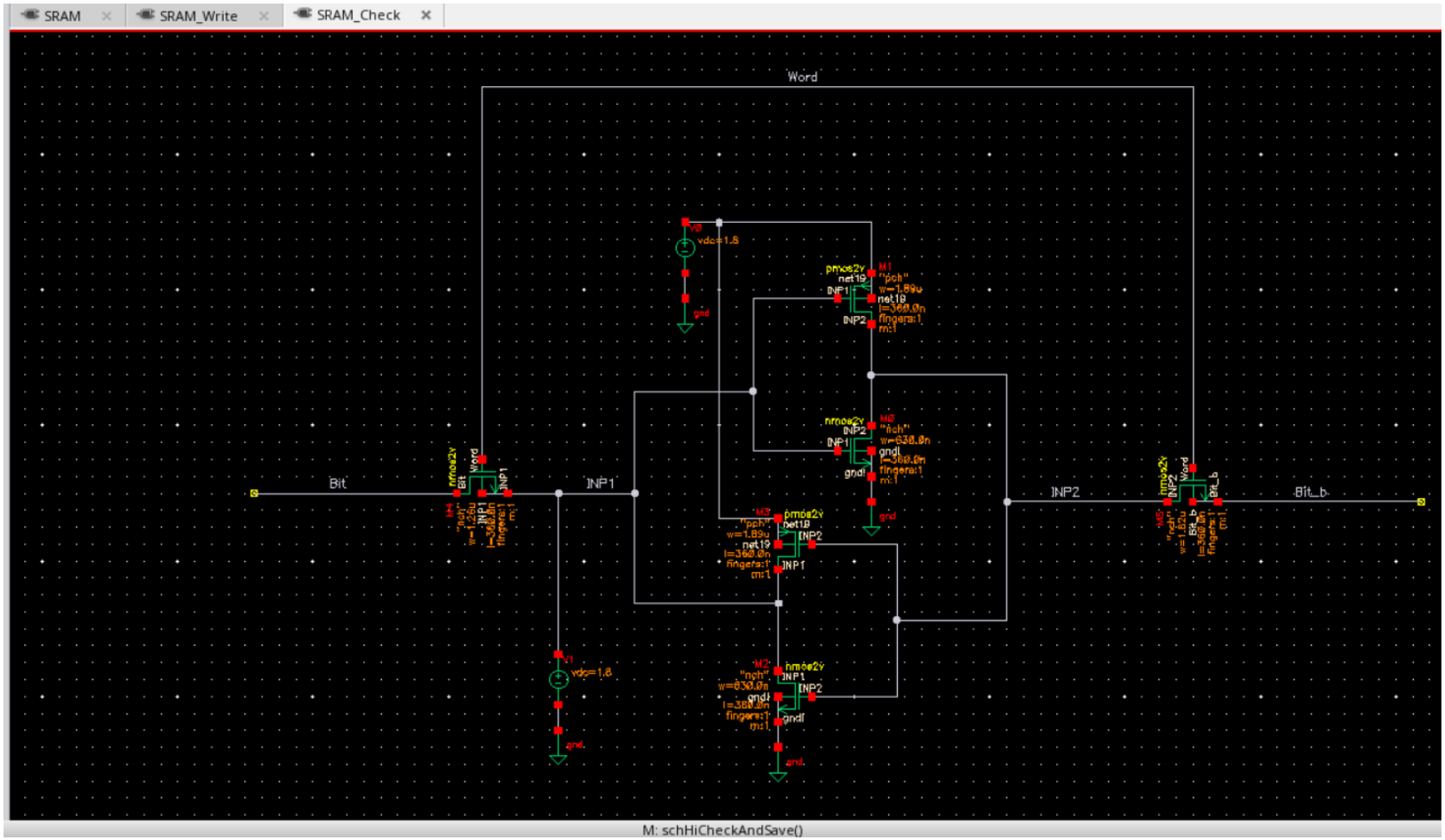
Schematic of SRAM

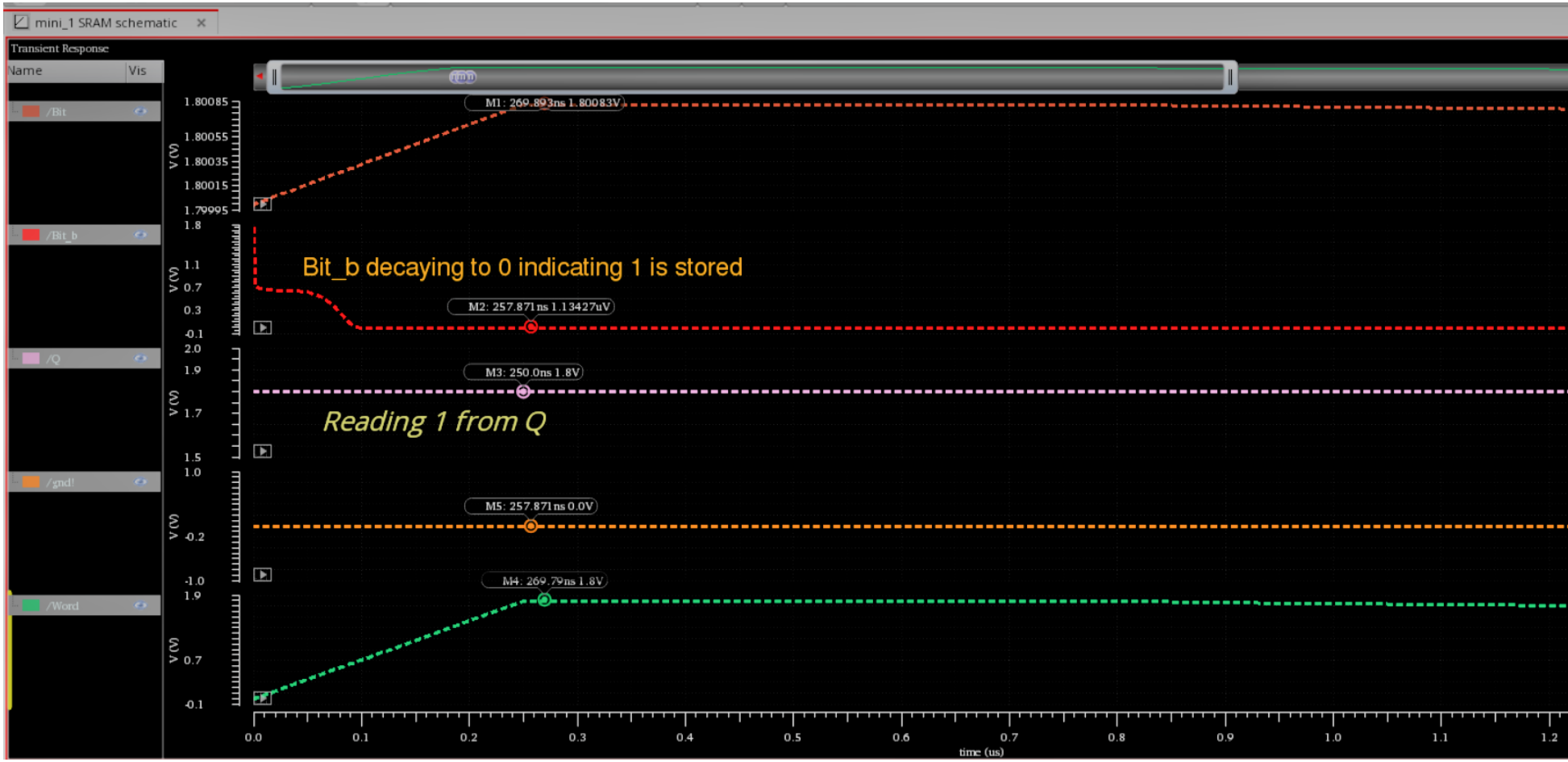


6T-SRAM consists of 2 Inverters and 2 Access transistors.

Choosing W/L of SRAM

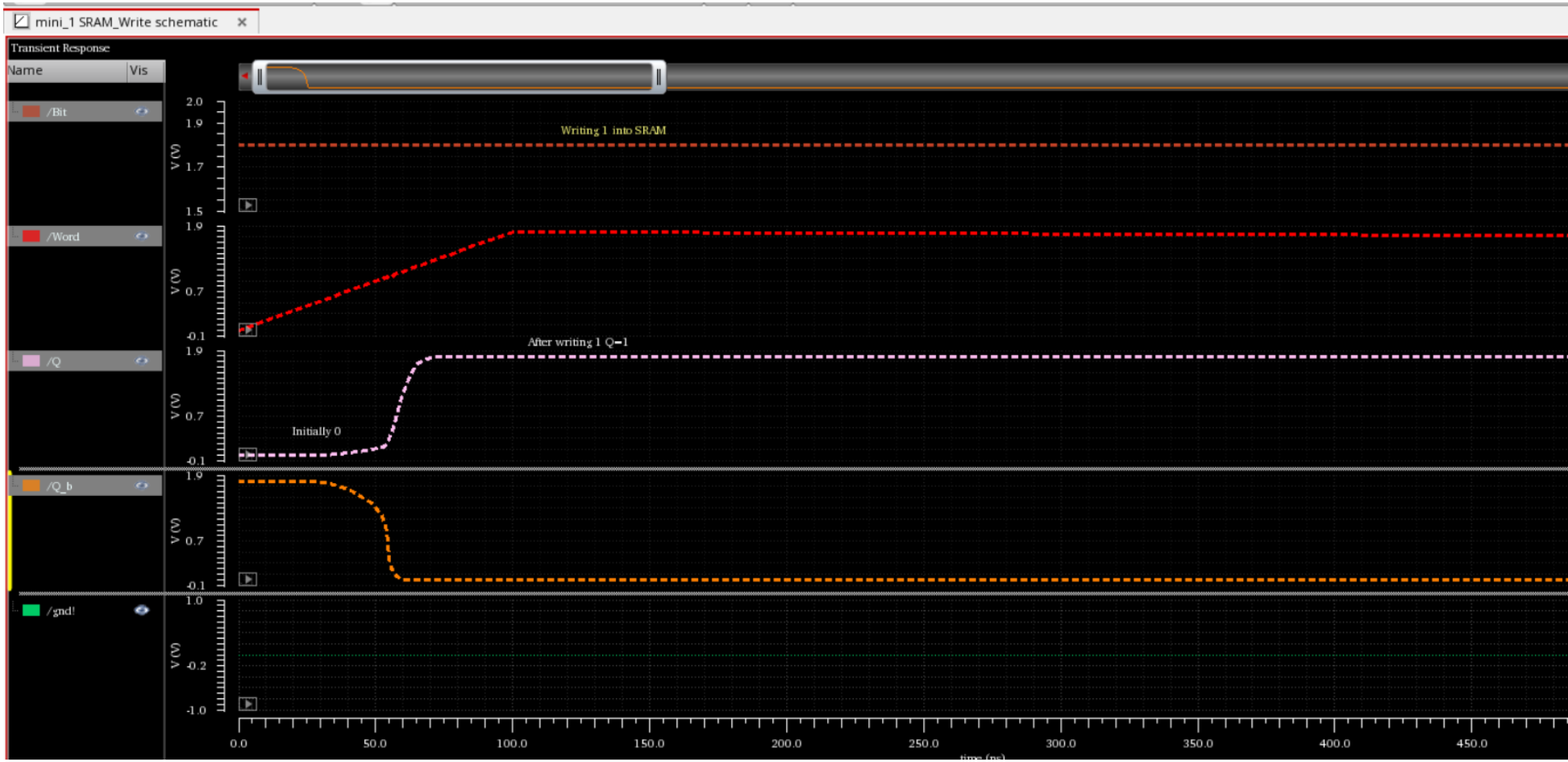
1. Assigned NMOS L= 360 nm W= 630 nm W/L=1.75.
2. For good functionality of the circuit strength of transistors should be in following order.
3. PULL DOWN Strength(D) > ACCESS Transistor(A) > PULL UP Strength(P).
4. Hence my PMOS(PULL UP) W/L is 3 times the W/L of NMOS(PULL DOWN).W=1890 nm and L=360 nm.
5. And ACCESS Transitor W/L is 2 times the W/L of NMOS(PULL DOWN).W=1260 nm and L=360 nm.

Read Operation



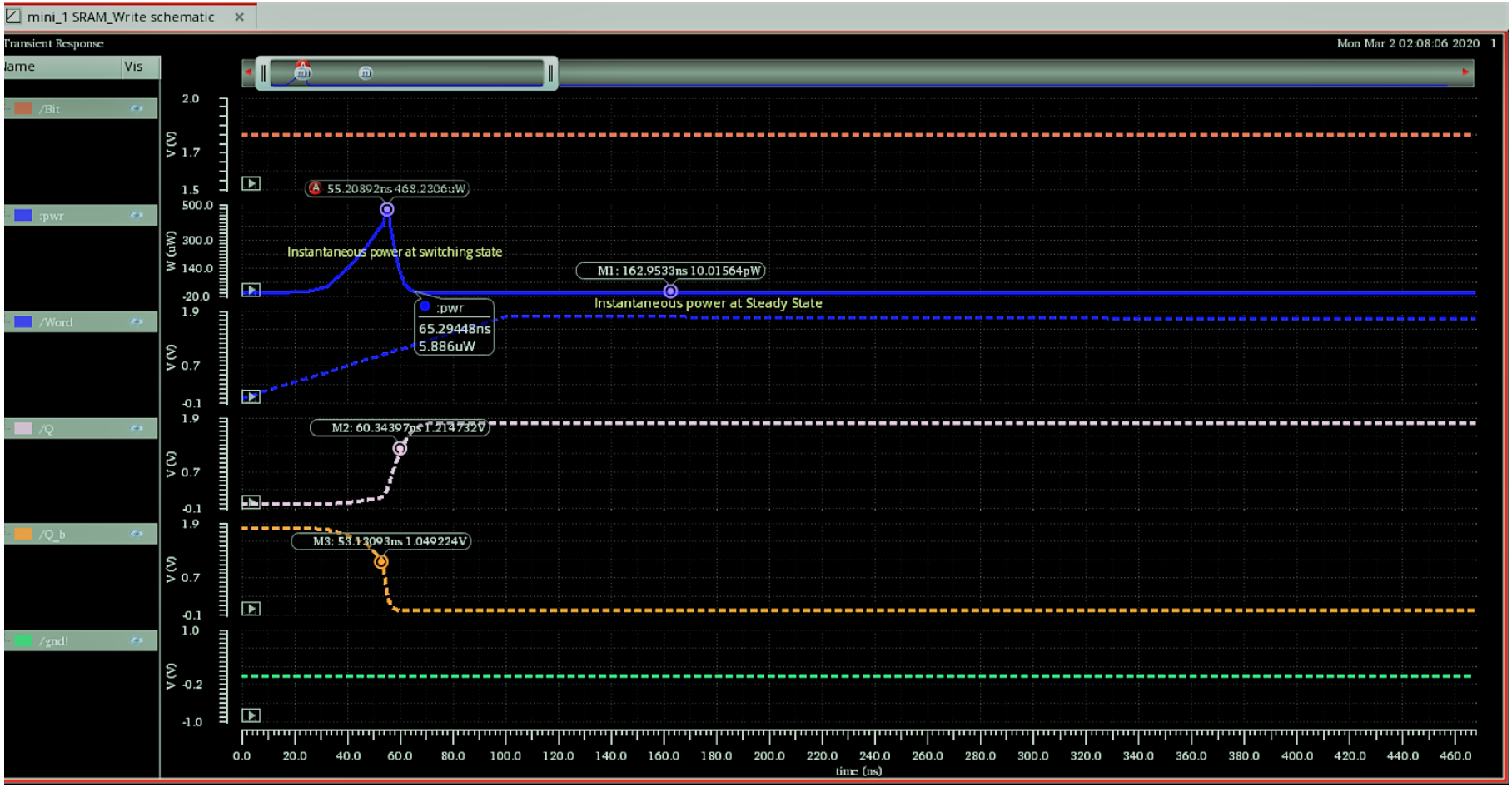
1. Initially 1 is stored. We need to read 1.
2. Initially both Bit and Bit-bar are precharged to high.
3. Here we can see that Bit-bar decays to 0 representing 1 is stored.

Write Operation



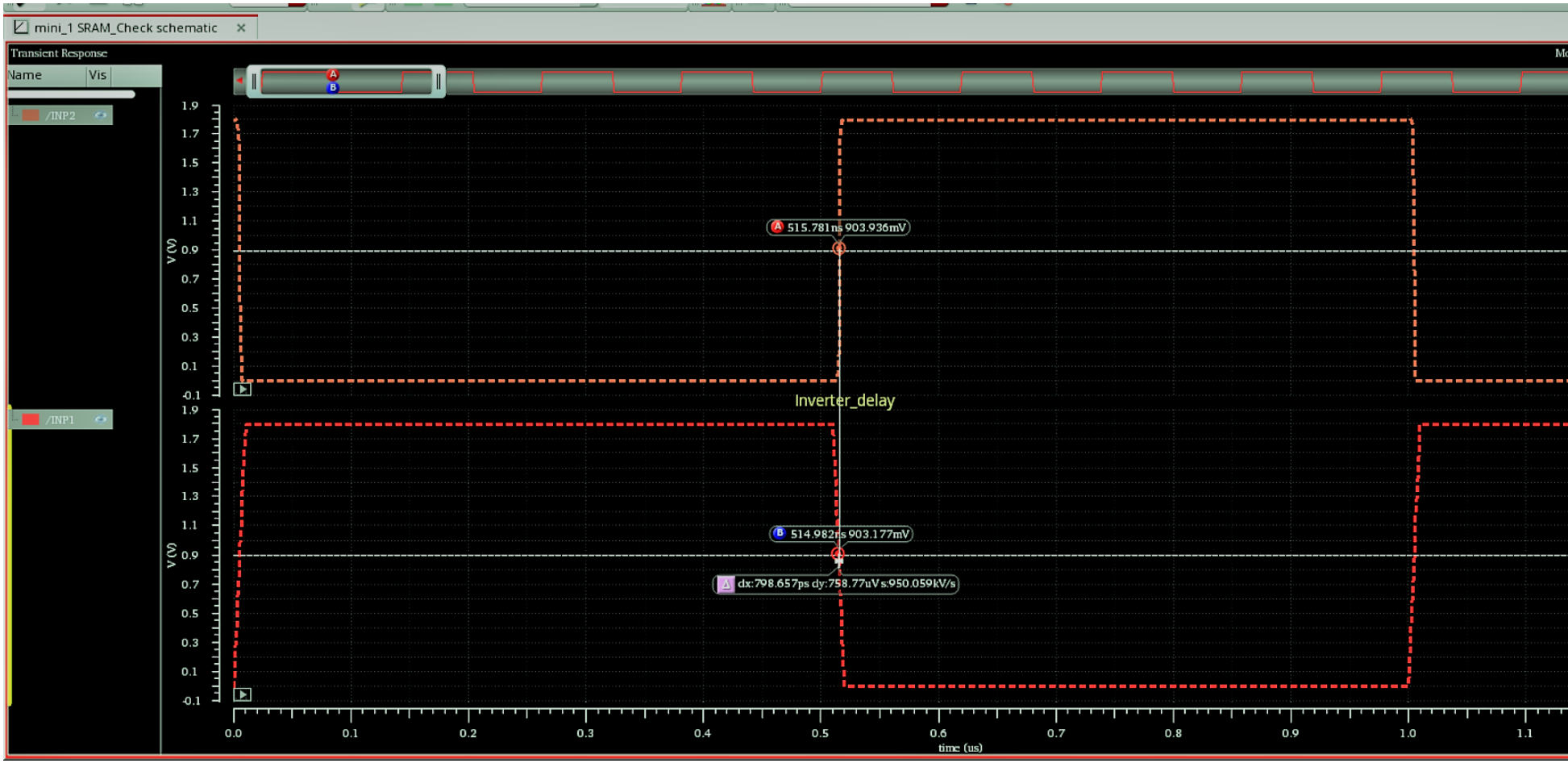
1. Initially 0 is stored in Q and 1 in Q-bar.
2. For writing we made Bit as 1 and Bit-bar as 0.
3. We can see that after Word bit reaches 1, 1 is stored in Q and 0 in Q-bar.

Instantaneous Power at switching and steady state



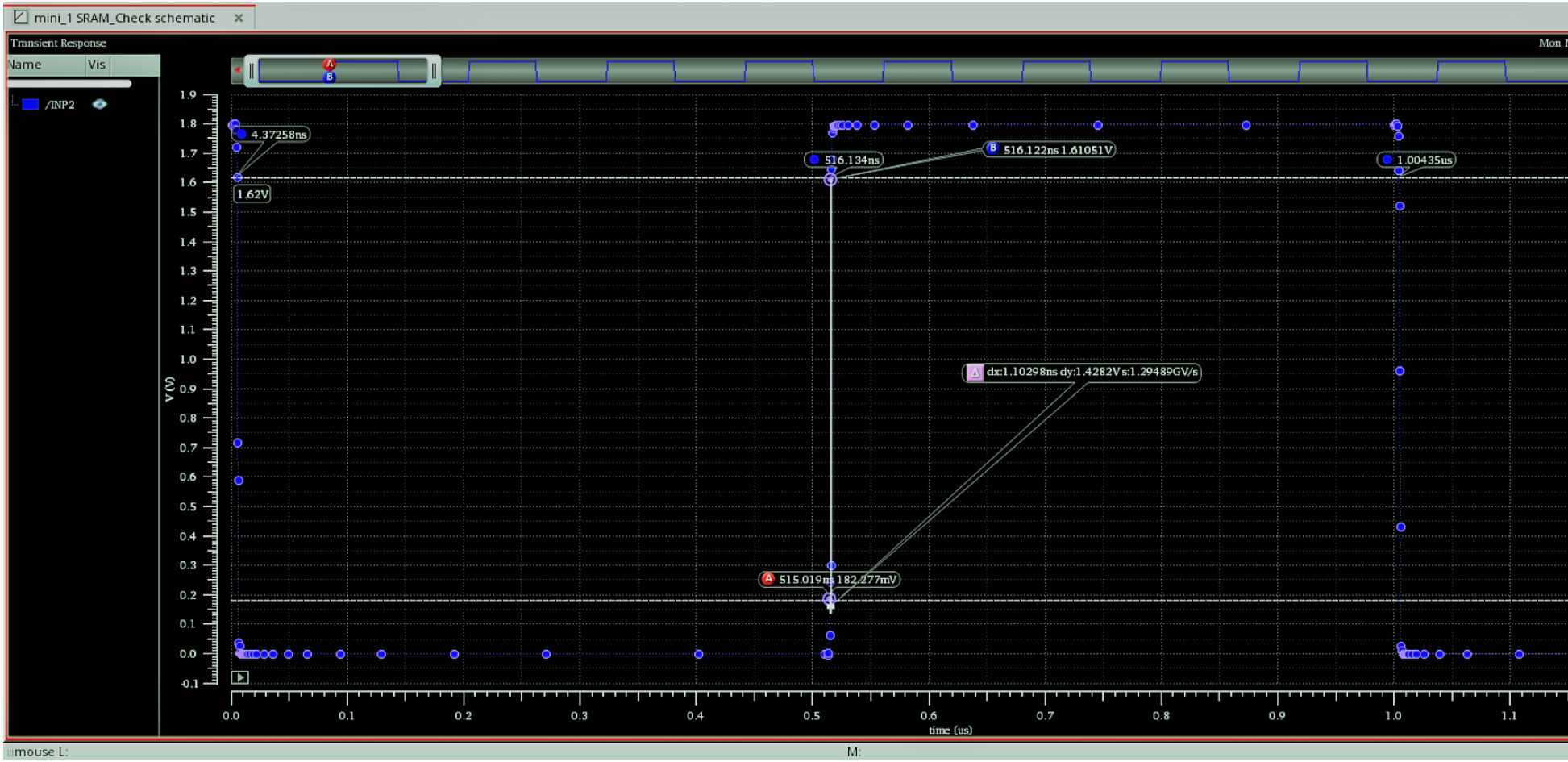
1. Here switching of Q happens from 0 to 1.
2. Switching instantaneous power is 468.23 μW.
3. Instantaneous power at steady state is 10.01564 pW.

Inverter Delay



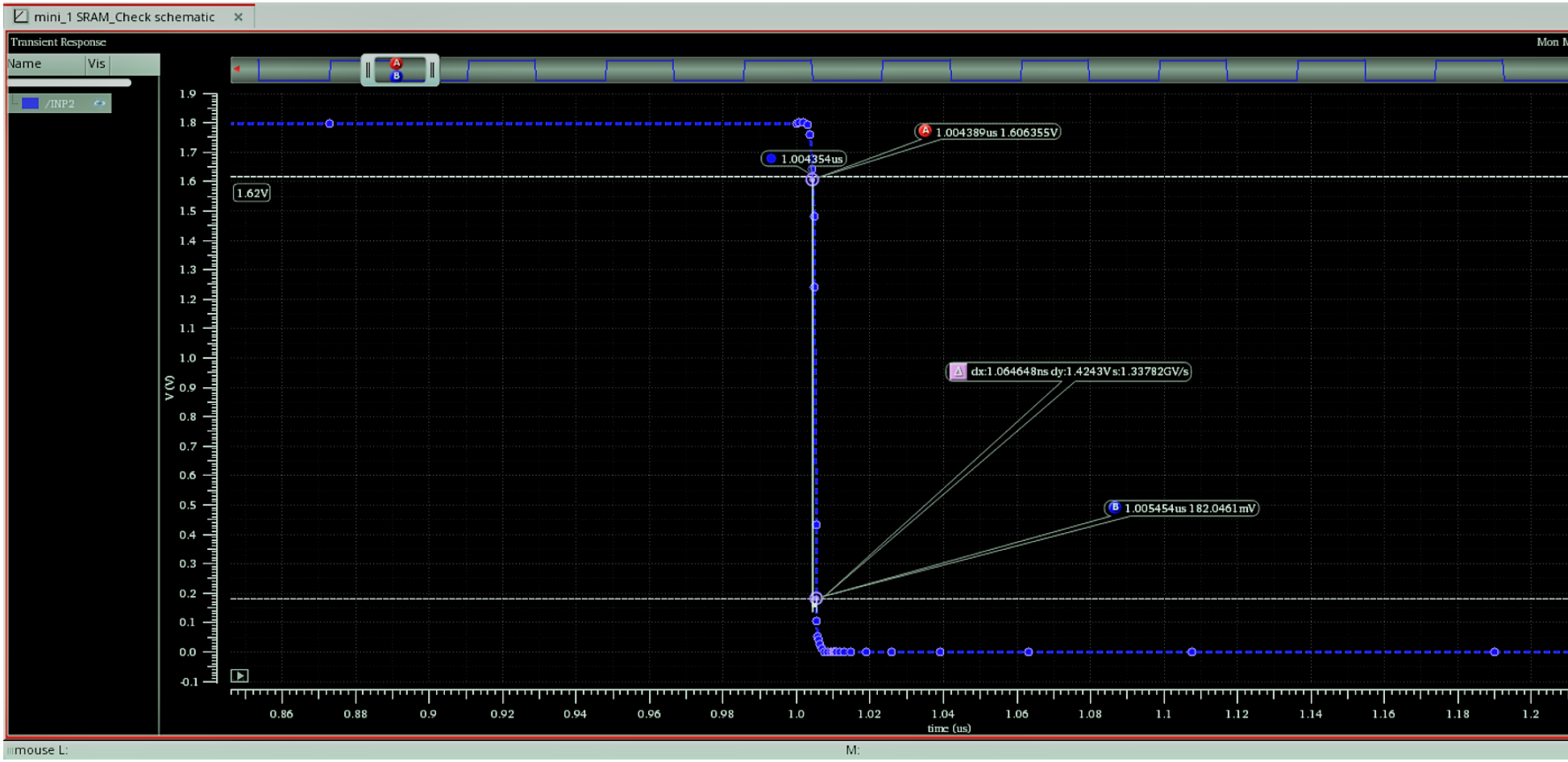
1. Inverter Delay here measured between 50% of input to 50% of output.
2. Inverter Delay here is 798.657ps.

Inverter Rise Time



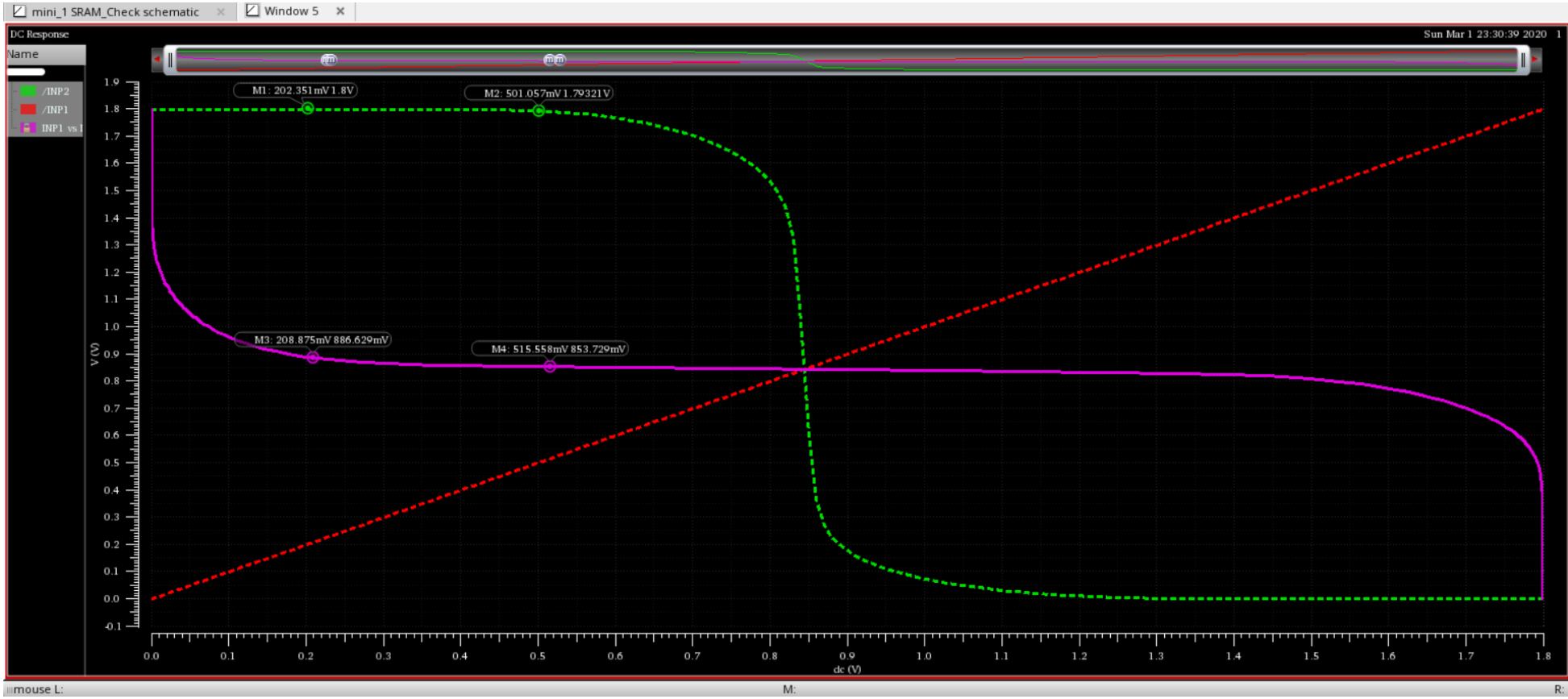
1. Inverter Rise here measured between 10% of maximum voltage and 90% of maximum voltage.
2. Rise time here is $1.10298ns$.

Inverter Fall Time



1. Inverter fall time here measured between 90% of maximum voltage and 10% of maximum voltage.
2. Fall time here is $1.064ns$.

Noise Margin of SRAM



1. The noise margin is calculated as length of this square depicted by markers.
2. Static Noise margin(SNM) =501.057 mV-202.351 mV = 298.706mV

Thank you