Characterisation of 2X4 and 3X8 Decoder

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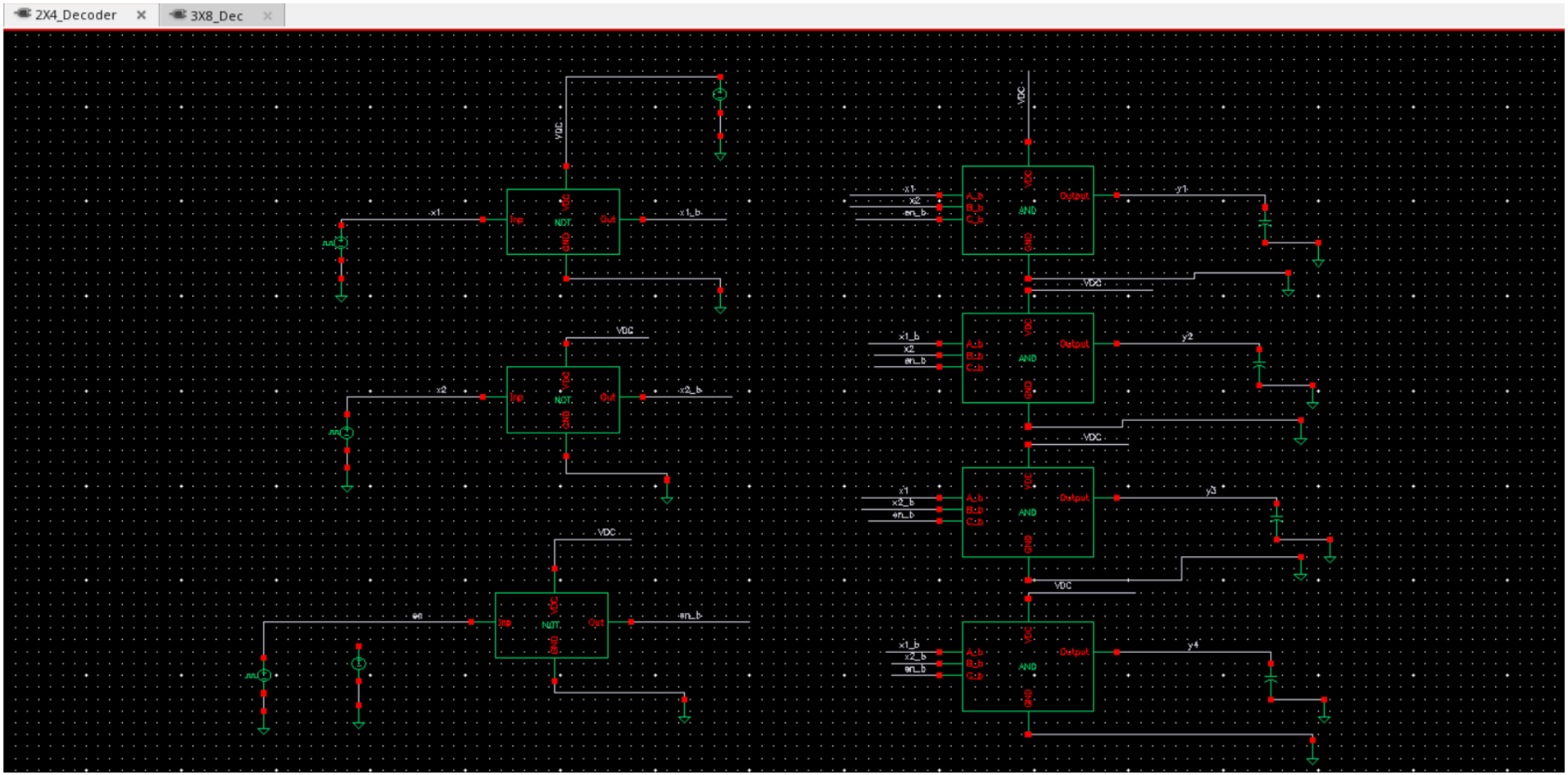
Schematic of 2X4 Decoder(Test Bench)



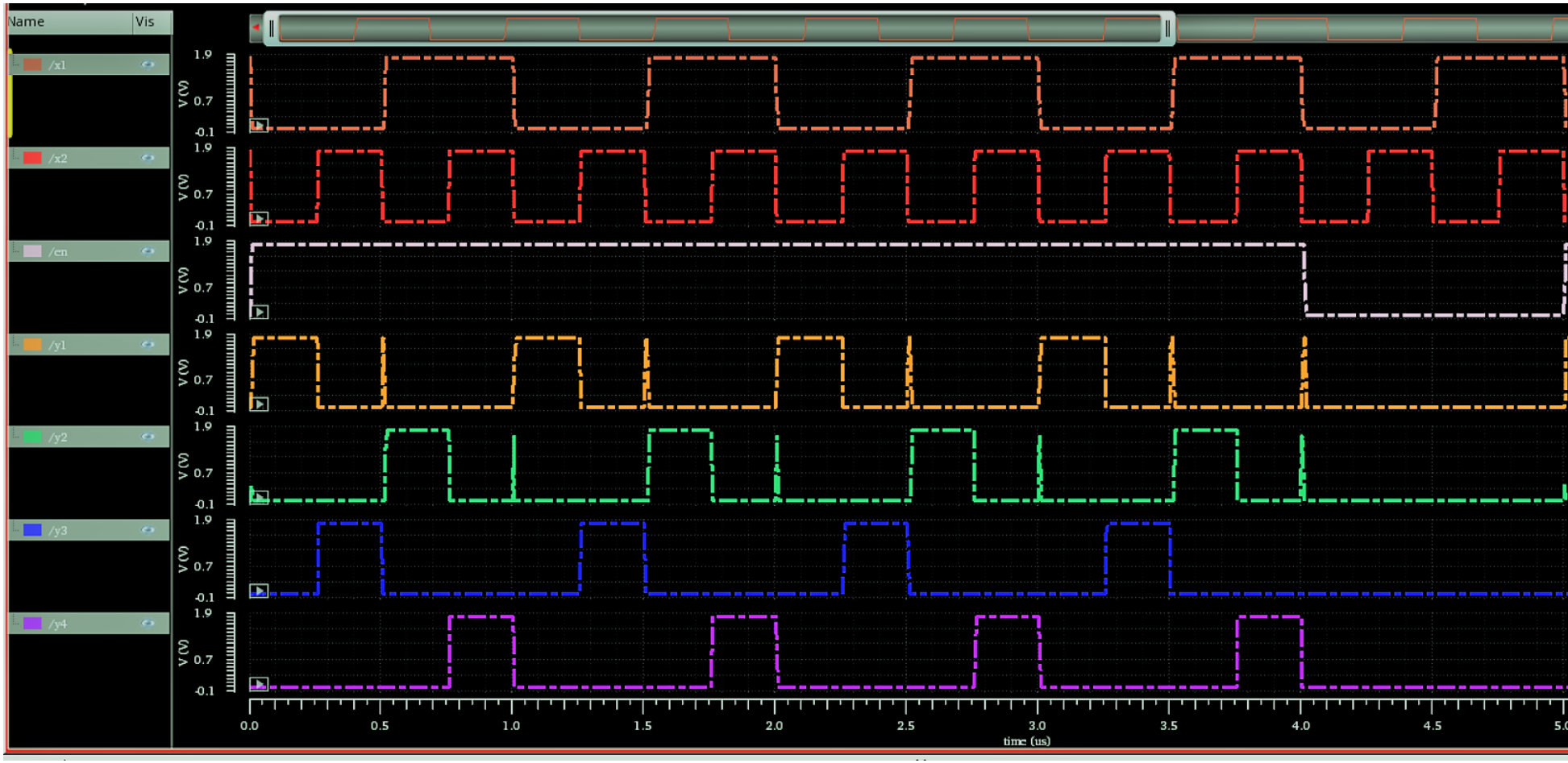
2X4 Decoder is made using 3 Inverters and 4 AND gates.
Total Number of transistors 3*(2 each for inverter) + 4*(6 each for AND gate).
Total of 30 transistors were used.

Modelling parasitic capacitances

1. C_{load} should drive 32 SRAM Cells.
2. Given Metal 1 Width=500 nm Length=100μm C_{ox}=895aF/μm
3. So, C_{load}= $C_{32SRAMcells}$+ $C_{M1-fringe}$ +$C_{M1-AreaCap}$
4. $C_{M1-fringe}$=C_{fringe}*$(2W + 2L)$
5. $C_{M1-area}$= C_{area}*W*L
6. $C_{32SRAMCELLS}$= $32 * C_{ox} * W$
7. $C_{load} \approx$ 38.1fF

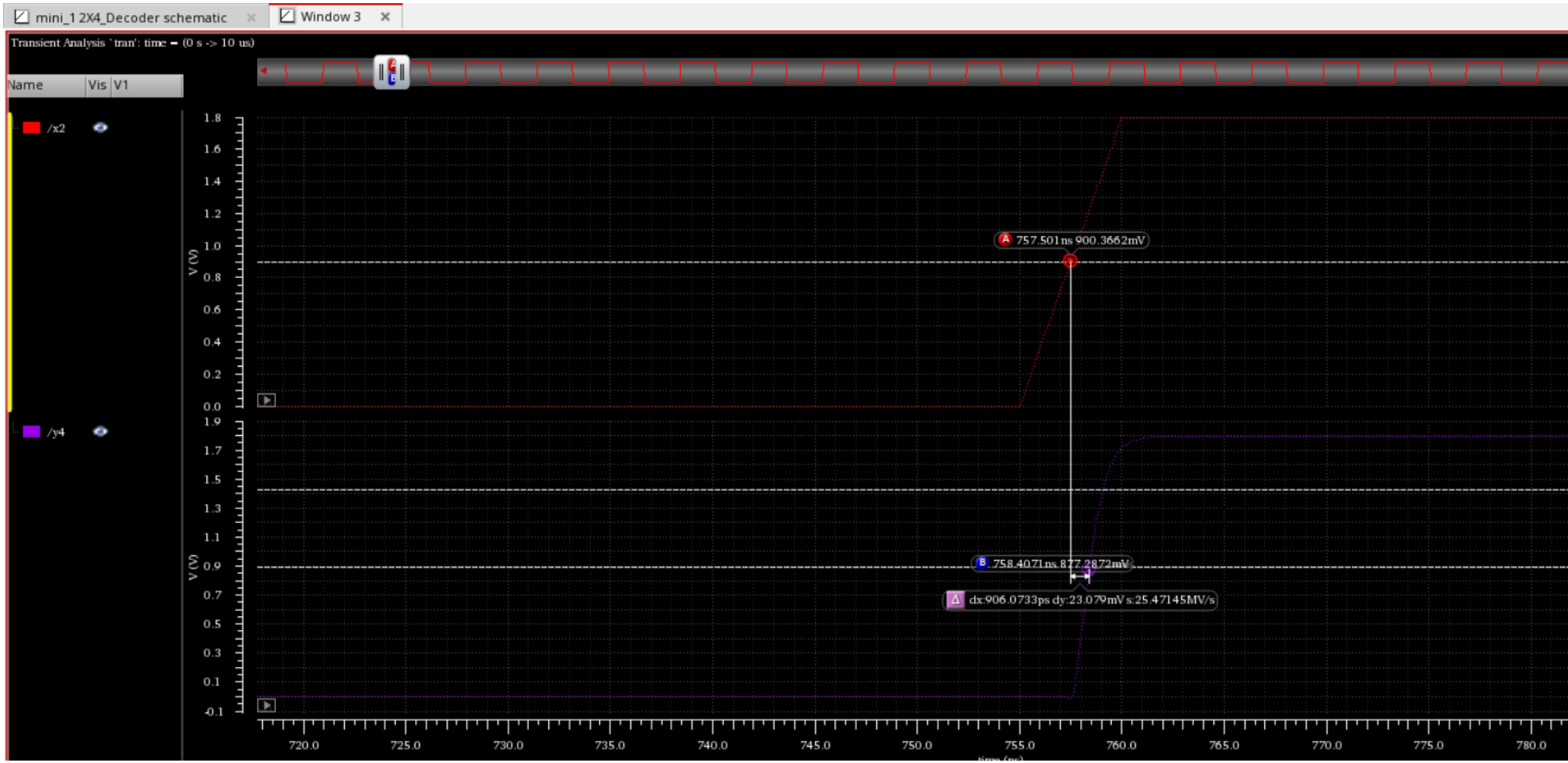
Using this parasitic capacitance at outputs, I simulated the decoder.

Transient Analysis for different combinations of inputs



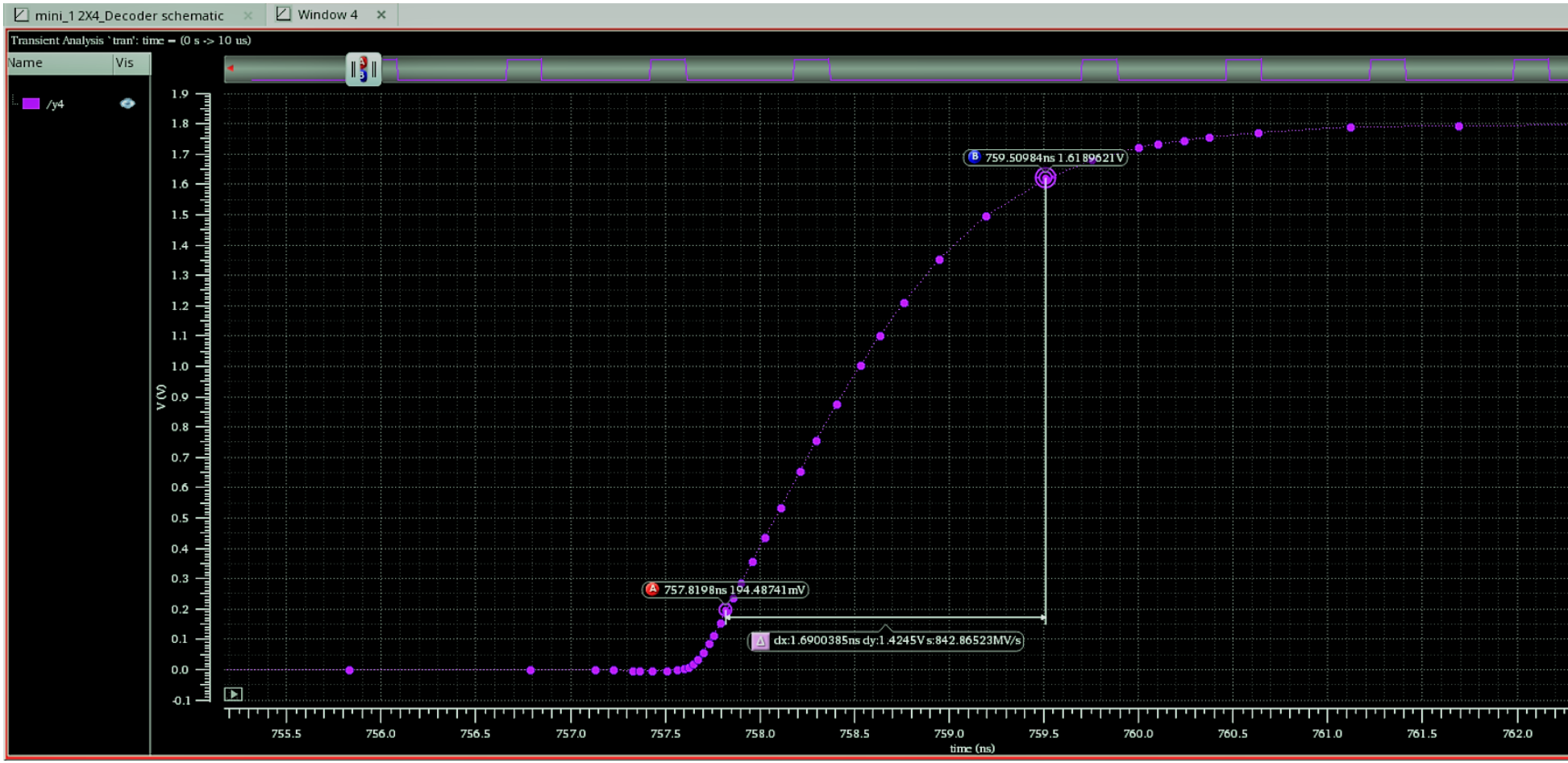
When enable is on, the functionality of decoder works, otherwise fails, which is shown in figure.

Delay for switching from WI(01) to WL(11)



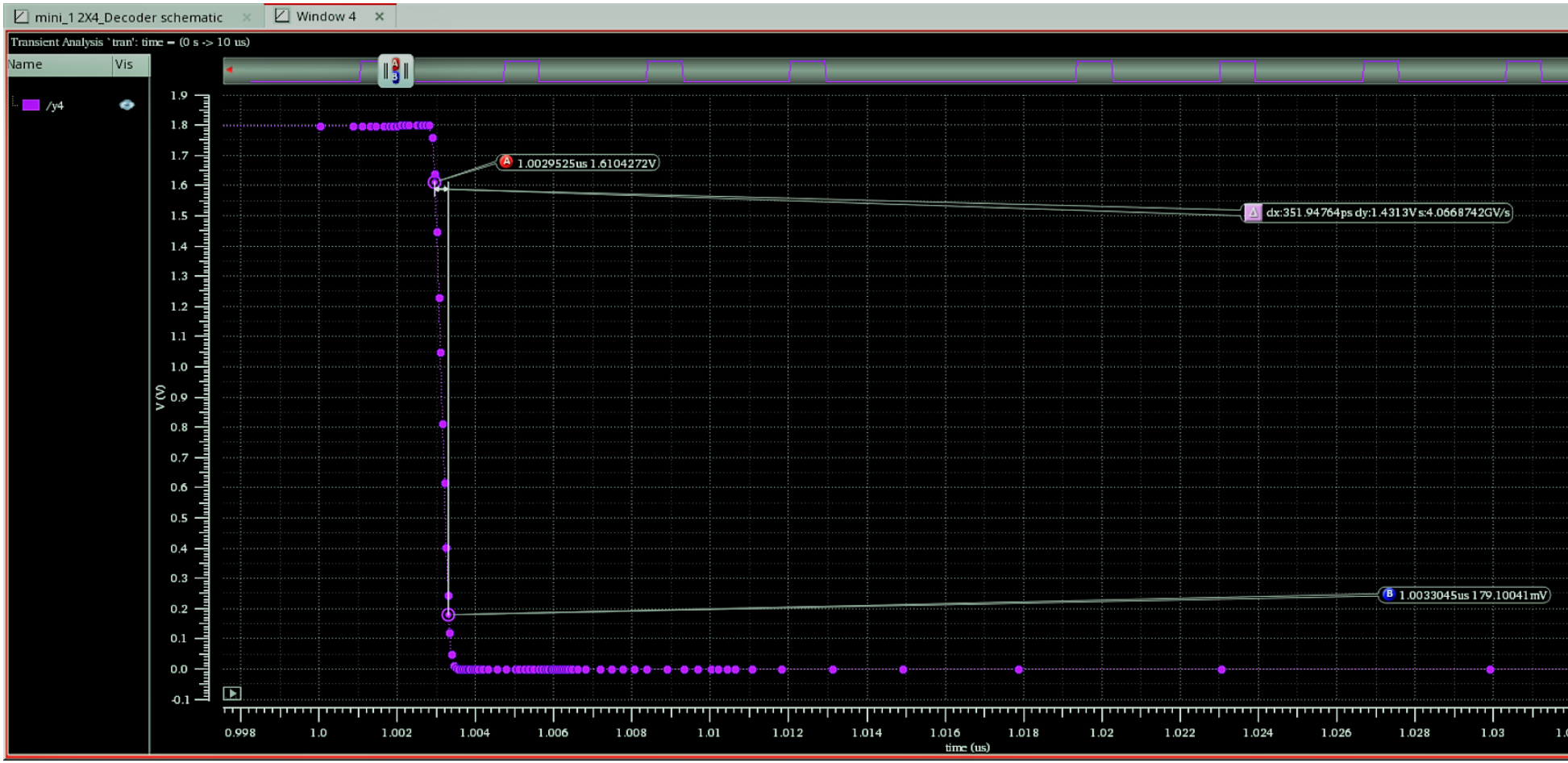
The delay is calculated as time diffeence between 50% of input to 50% of output. The delay is 906ps.

Rise time



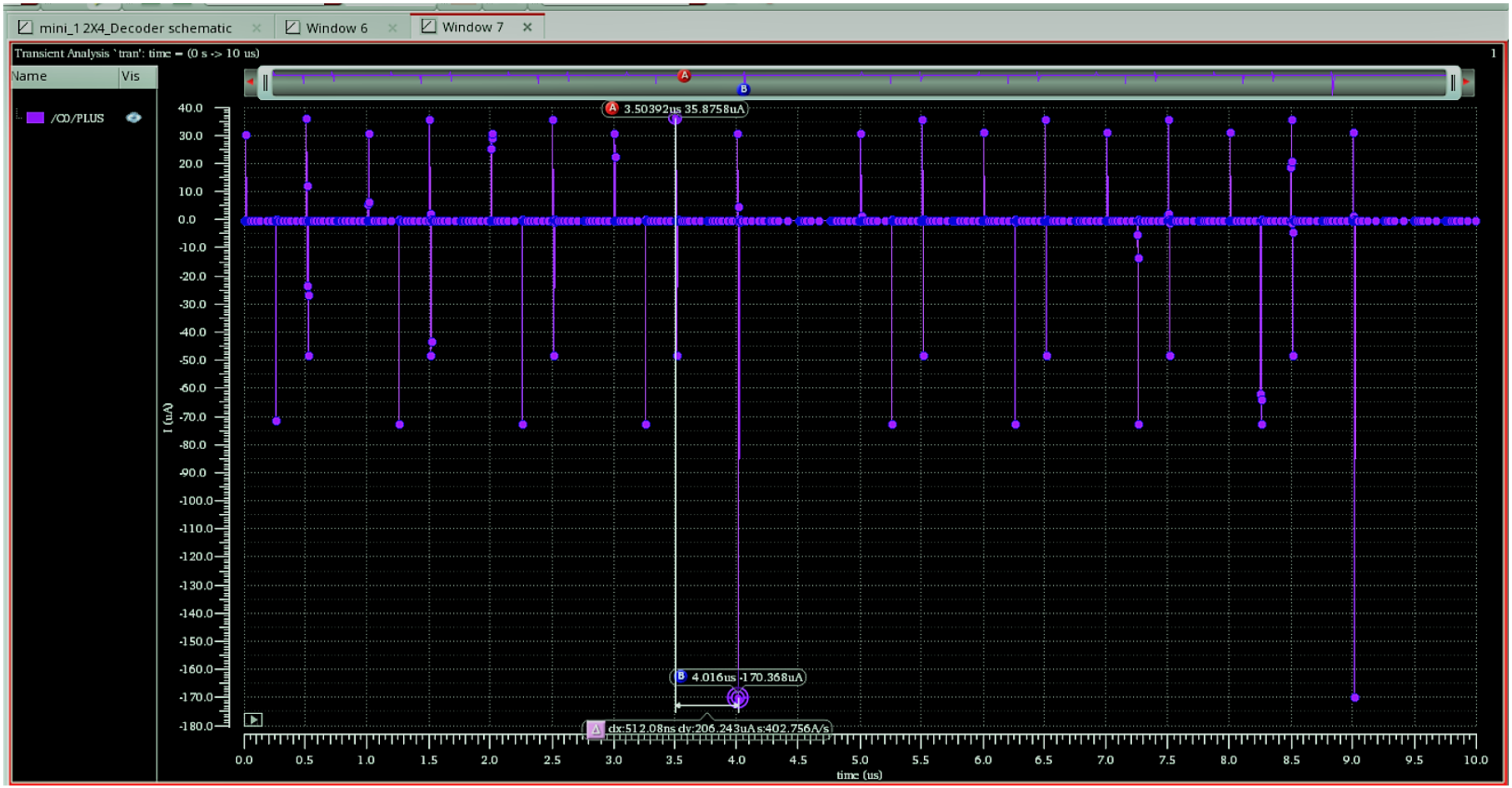
The rise time is calculated as time difference between 10% of maximum voltage and 90% of maximum voltage. The rise time is 1.69ns.

Fall time



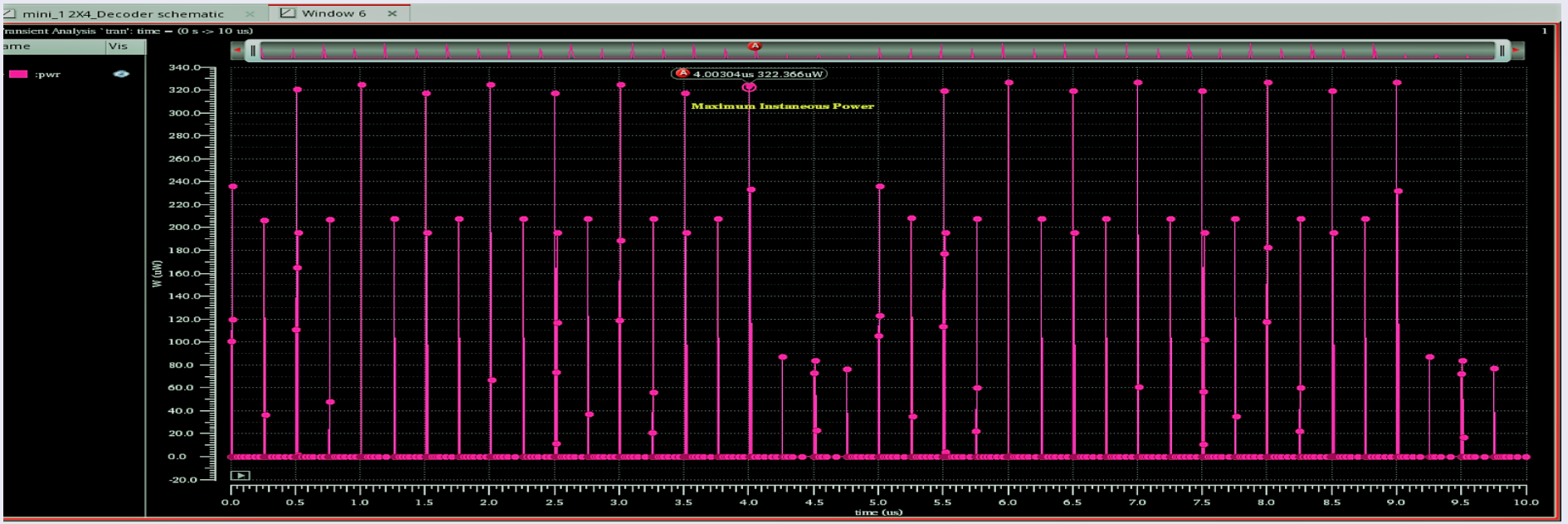
The fall time is calculated as time difference between 90% of maximum voltage and 10% of maximum voltage. The fall time is 351.9ps.

Instantaneous current

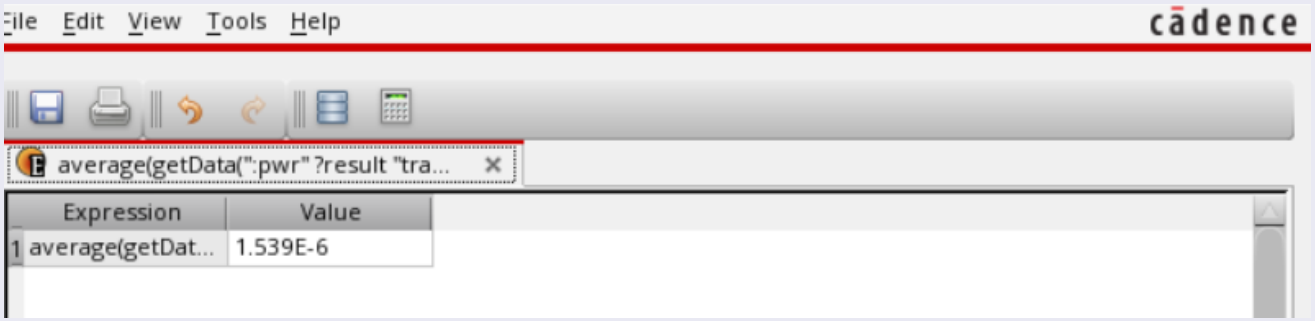


The maximum and minimum current are shown as A and B.

Instantaneous Power and average power

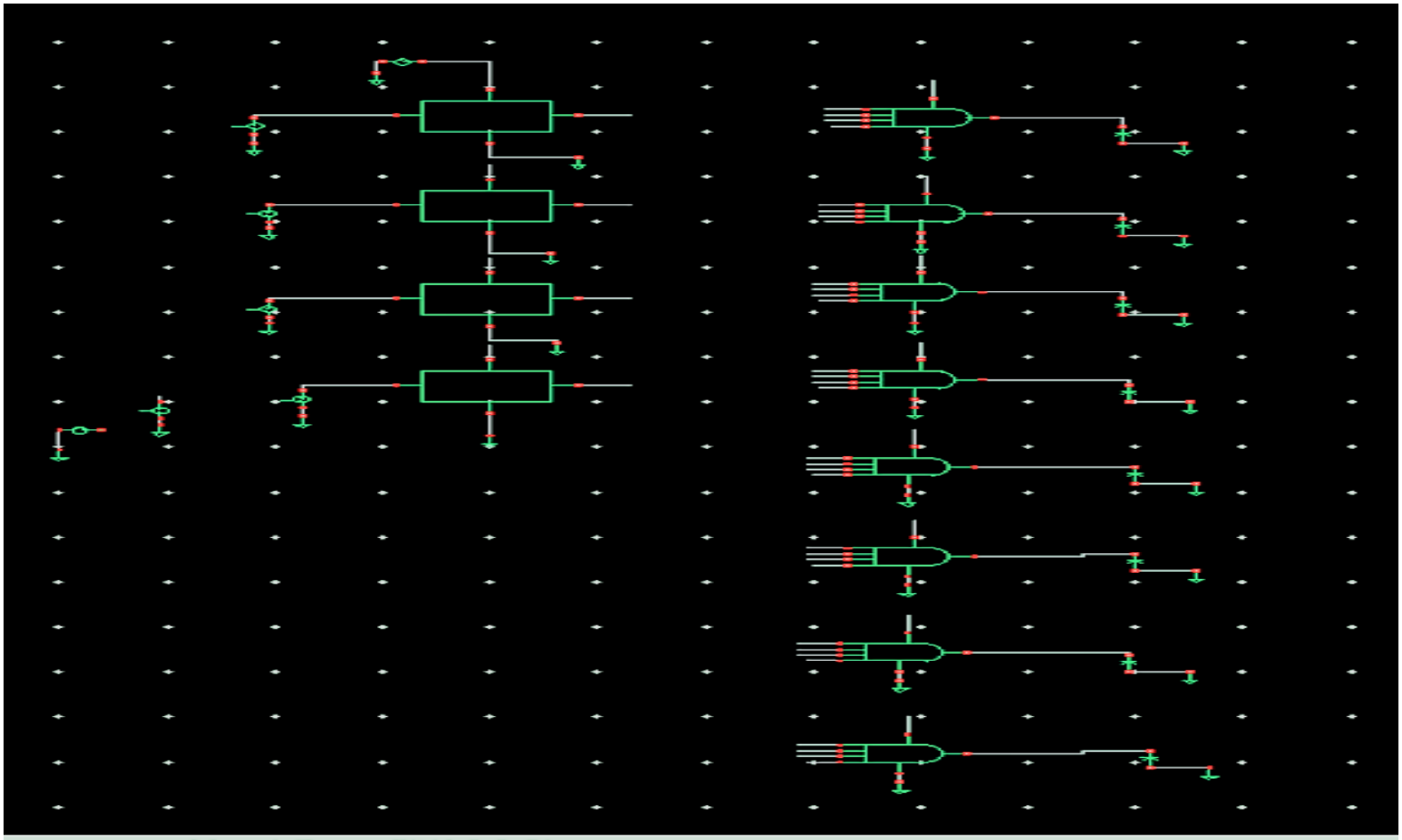


The maximum Instantaneous power is 322.366μ W .



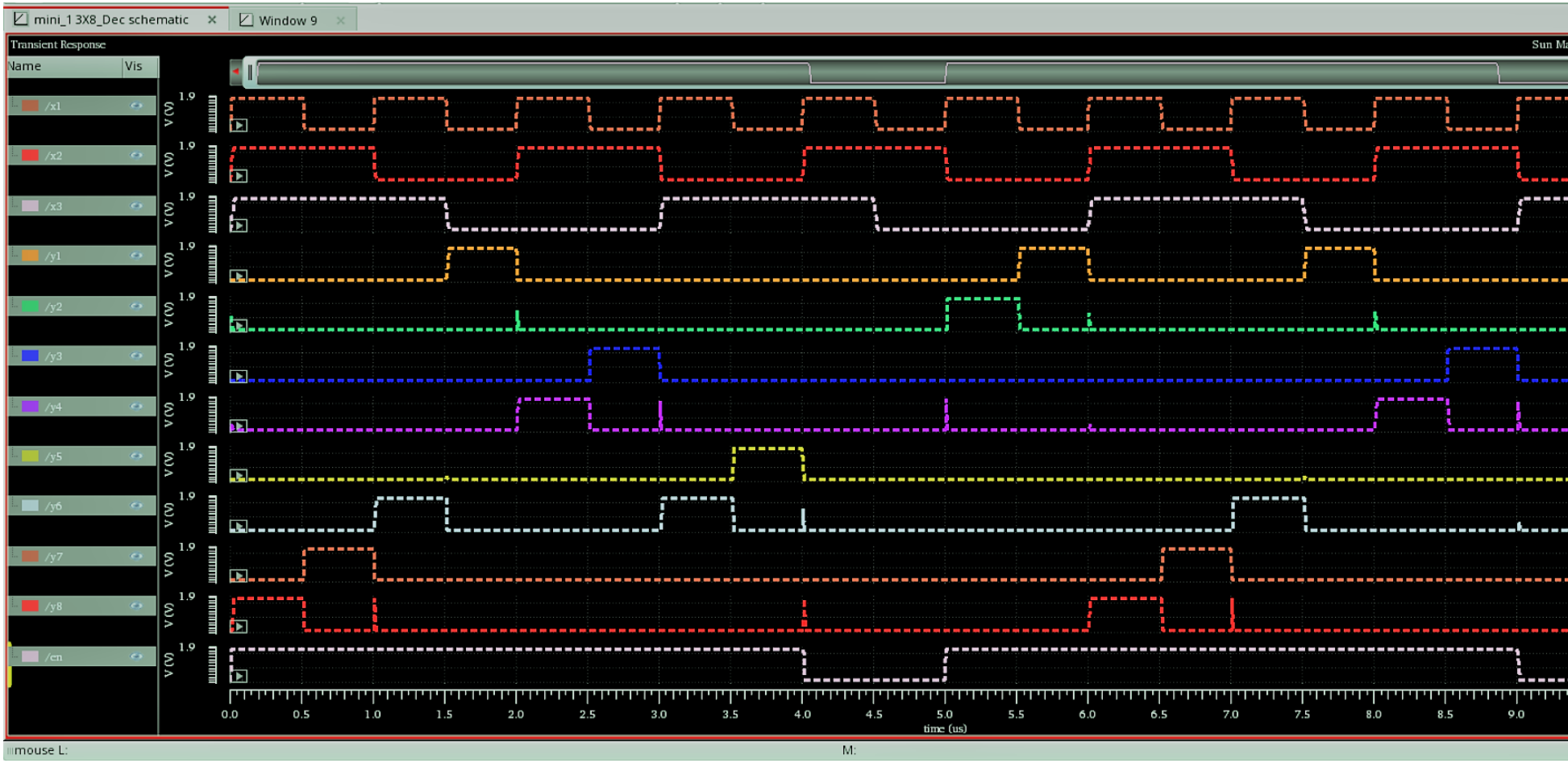
The Average power is 1.539μ W.

Schematic of 3X8 Decoder(Test Bench) with enable



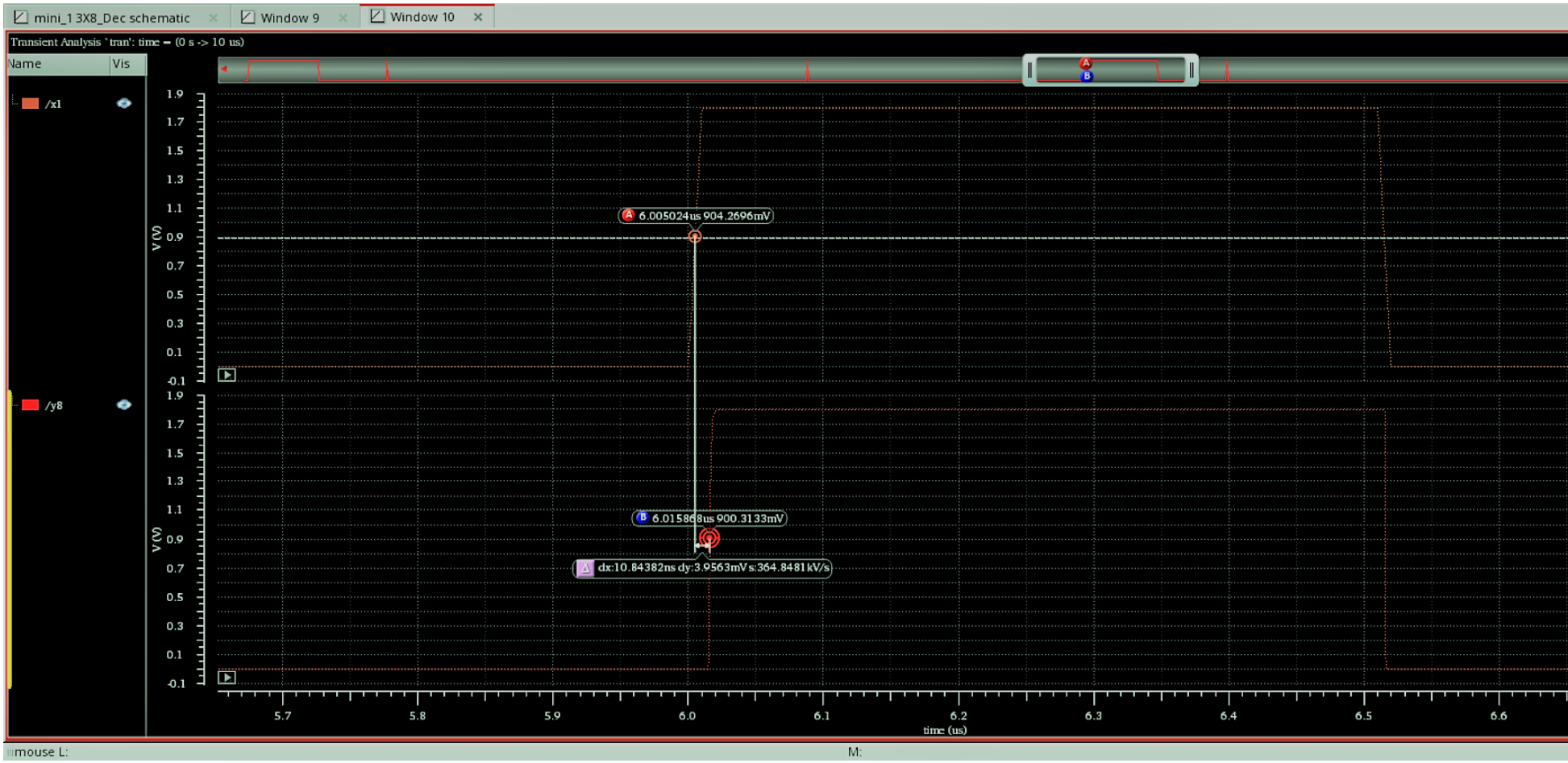
2X4 Decoder is made using 4 Inverters and 8 AND gates.
Total Number of gates 4*(2 each for inverter) + 8*(8 each for AND gate).
Total of 72 gates were used.

Transient Analysis for different combinations of inputs



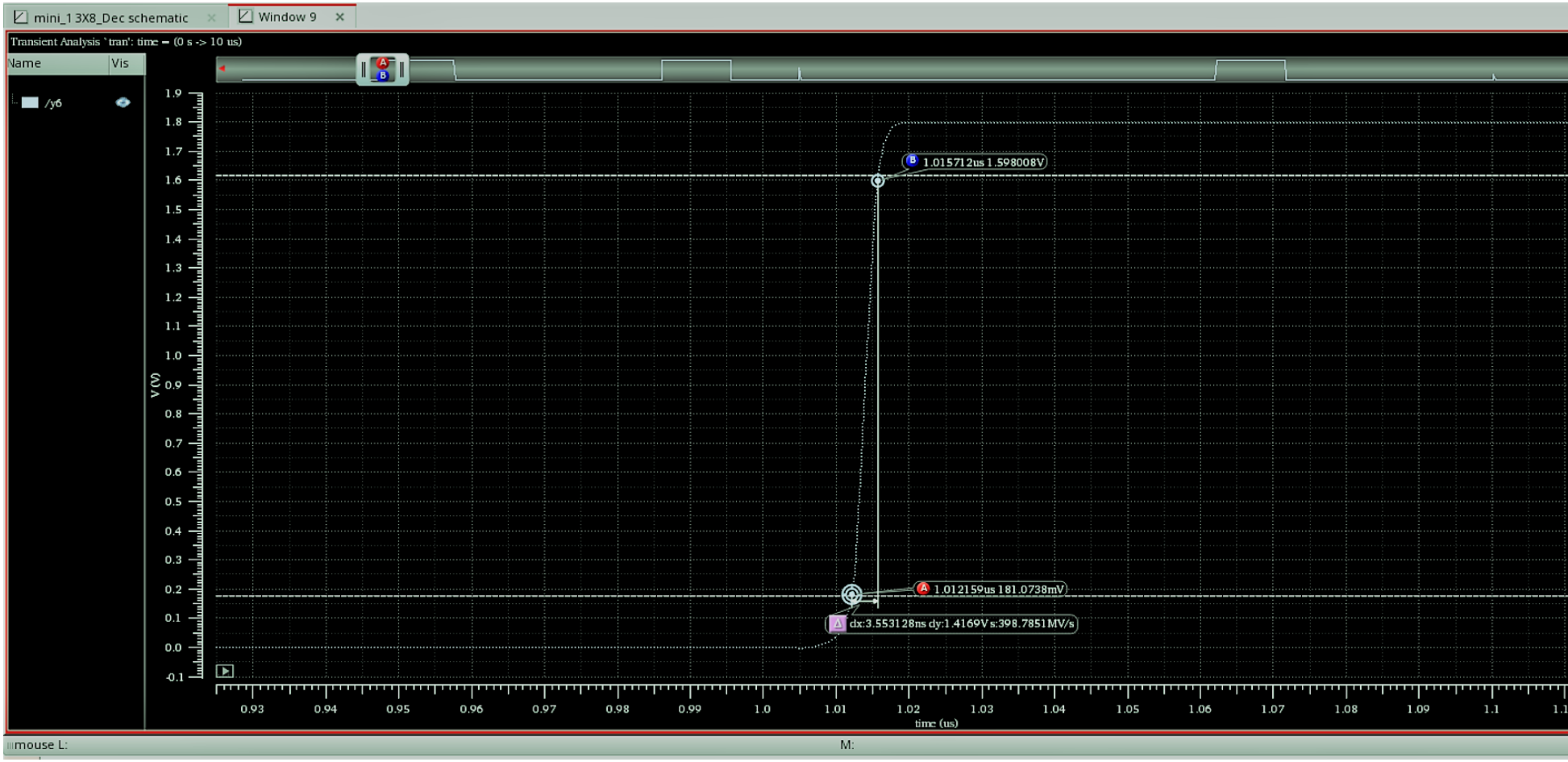
When enable is on, the functionality of decoder works, otherwise fails, which is shown in figure.

Delay for switching from WI(011) to WL(111)



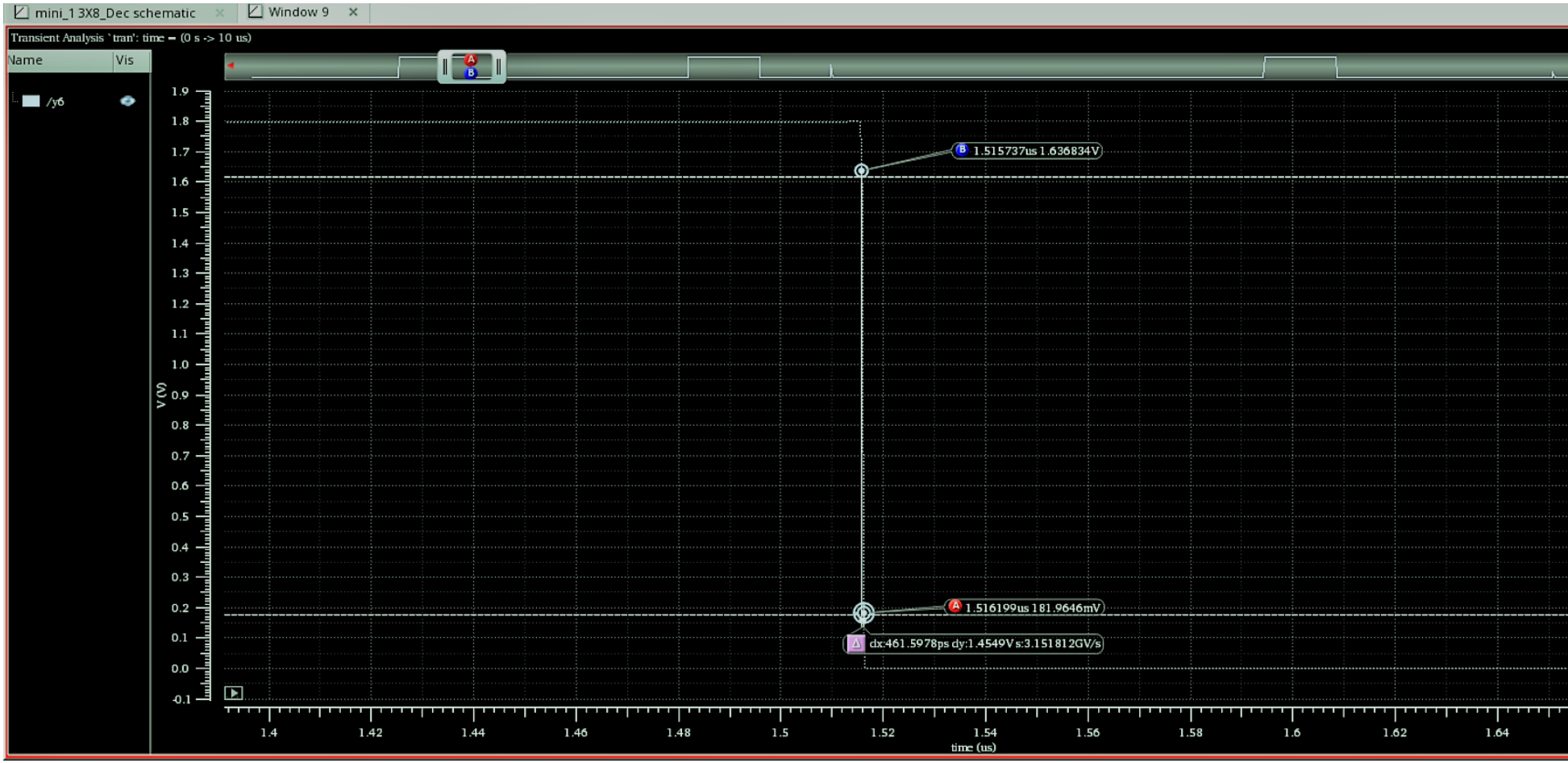
The delay is calculated as time diffeence between 50% of input to 50% of output. The delay is 10.84ns.

Rise time



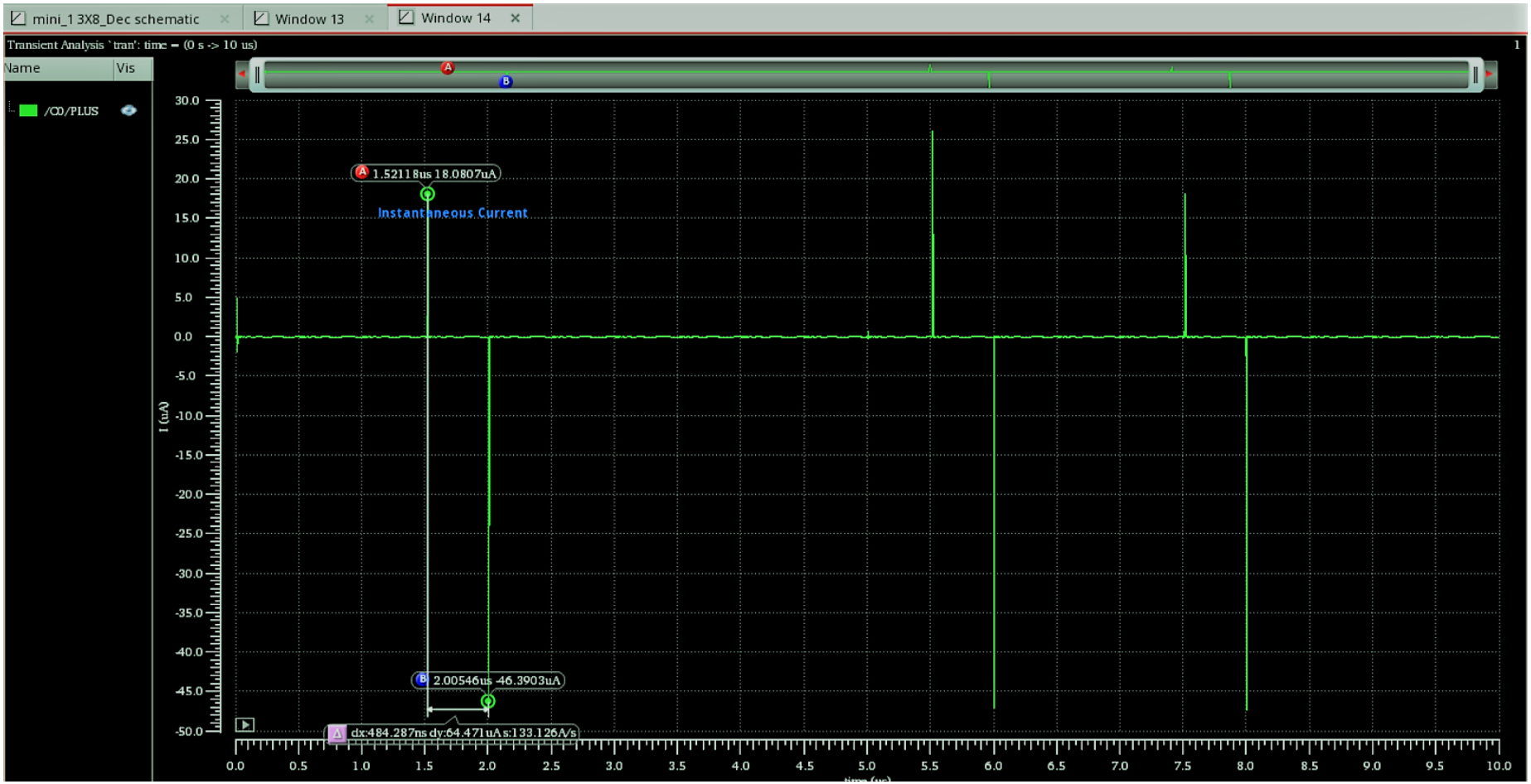
The rise time is calculated as time difference between 10% of maximum voltage and 90% of maximum voltage. The rise time is 3.5ns.

Fall time



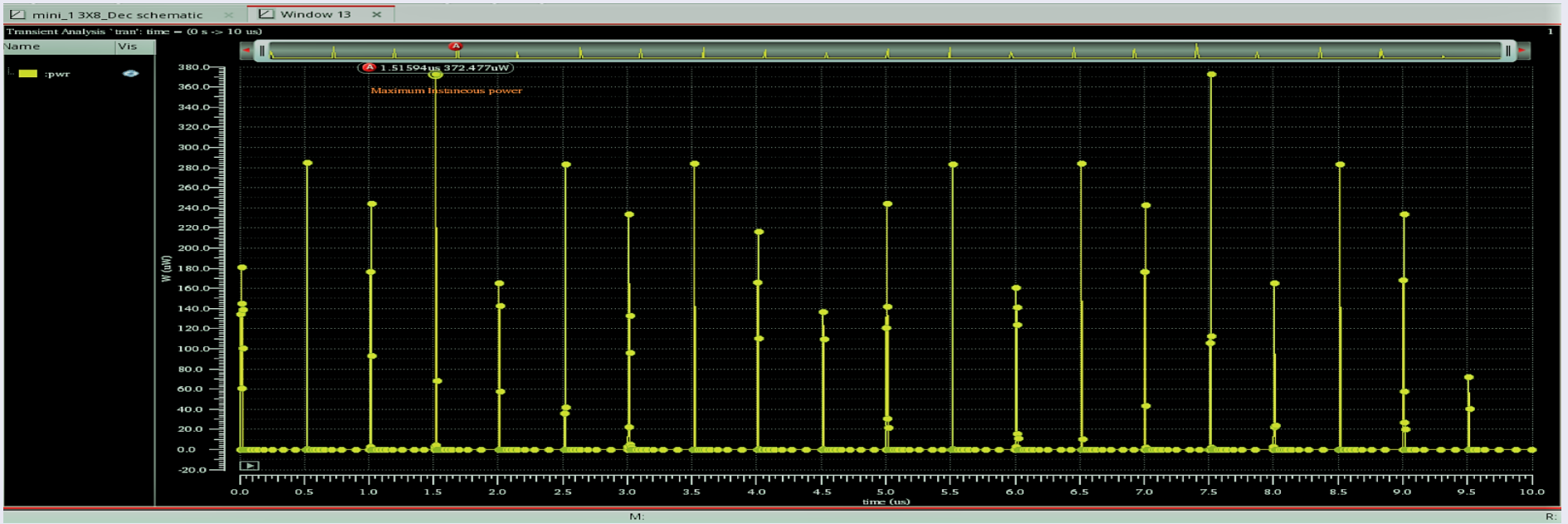
The fall time is calculated as time difference between 90% of maximum voltage and 10% of maximum voltage. The fall time is 461.59ps.

Instantaneous current

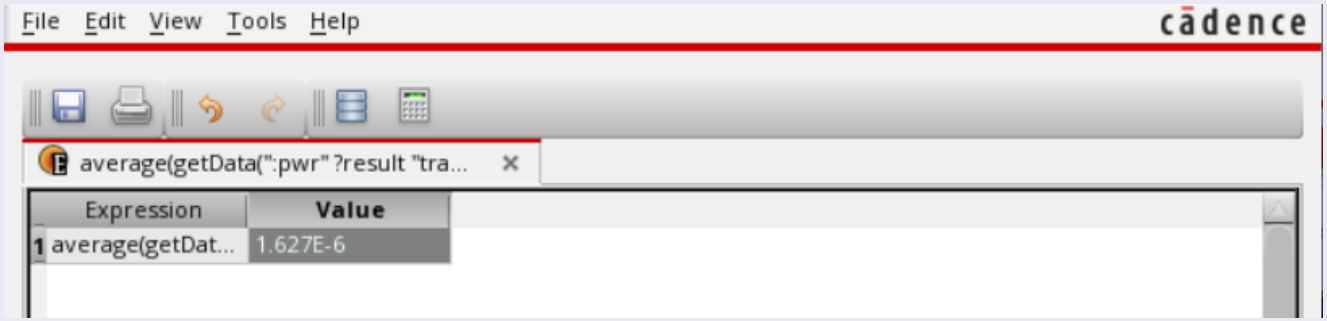


The maximum and minimum current are shown as A and B.

Instantaneous Power and average power



The maximum Instantaneous power is 372.477μ W .



The Average power is 1.627μ W.

Thank you