Characterisation of 6T-SRAM Memory Array

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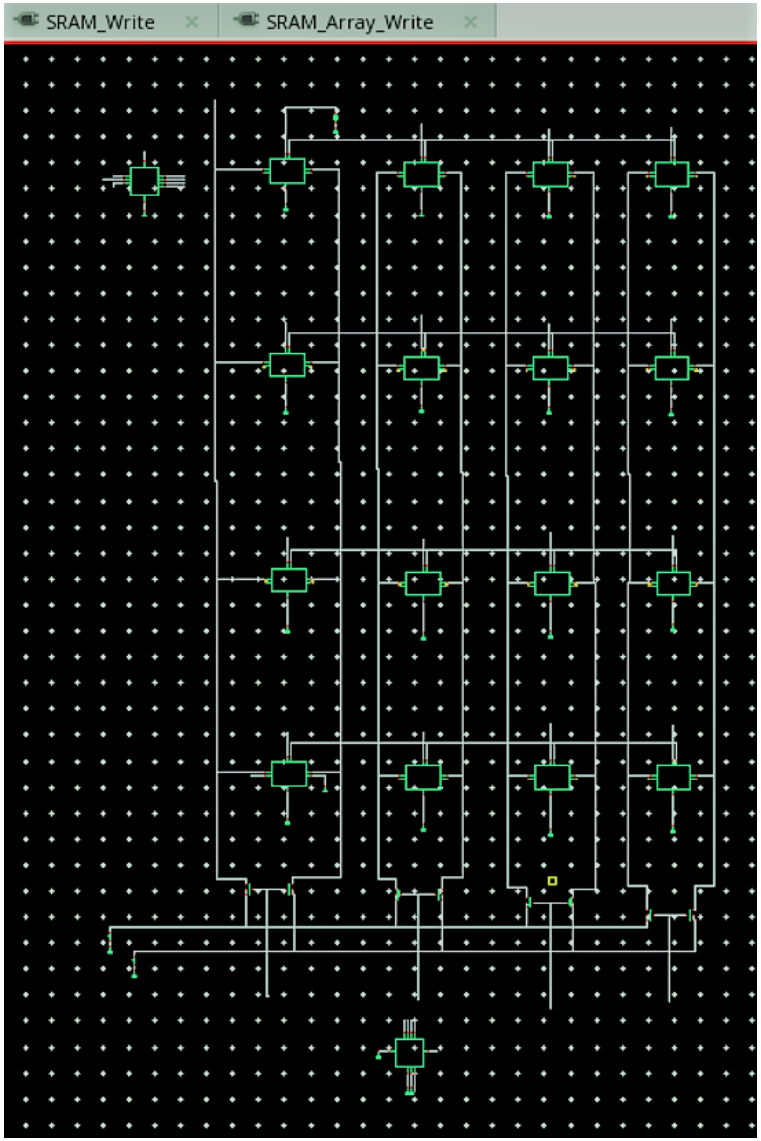
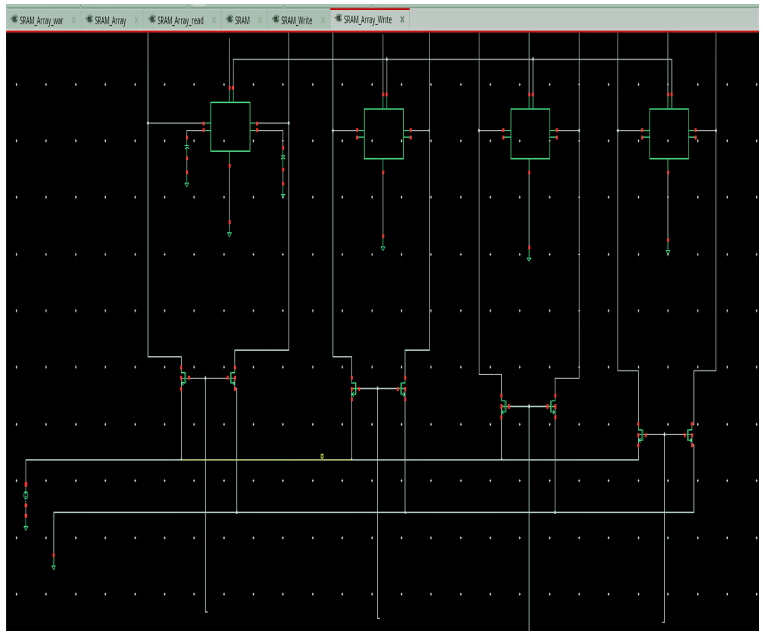
Schematic of Memory Array

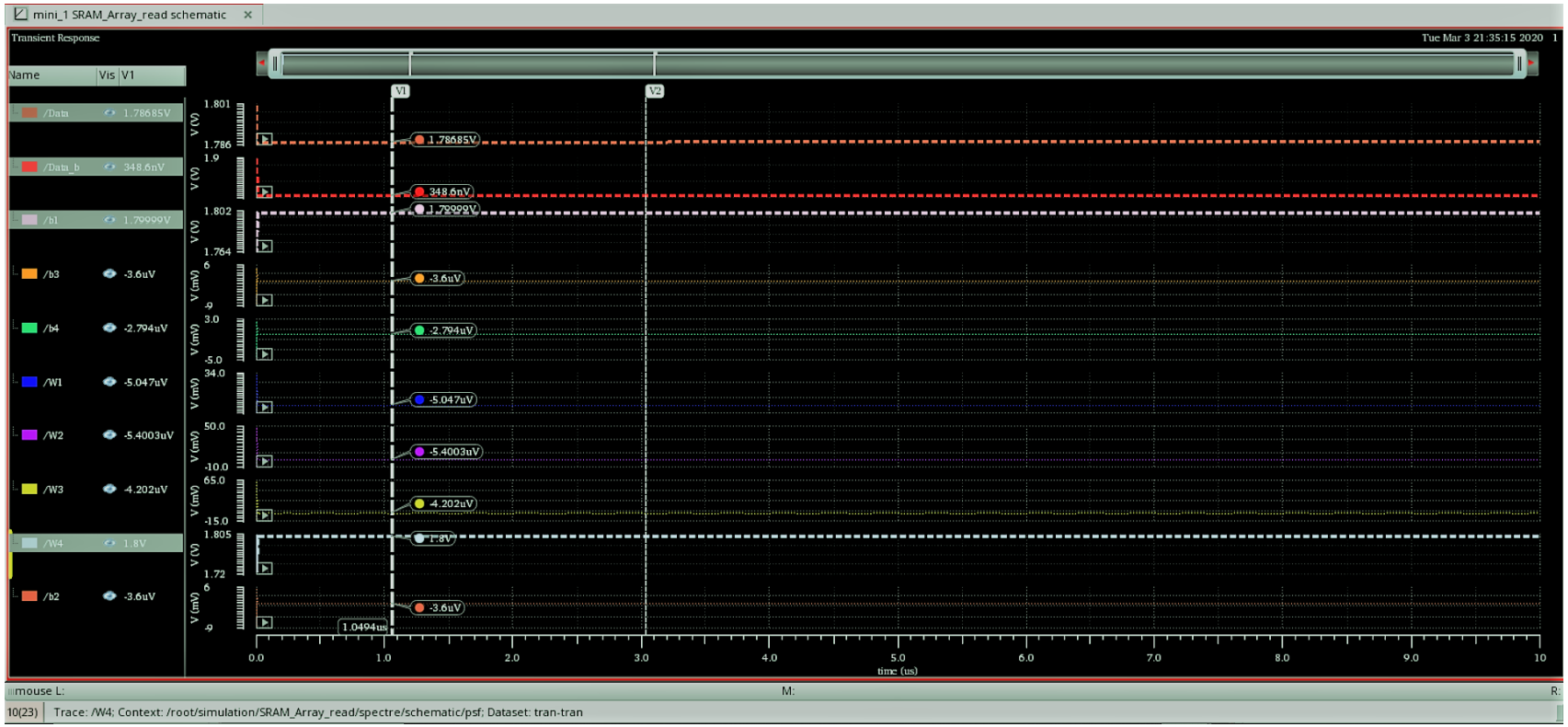




Working of Memory Array

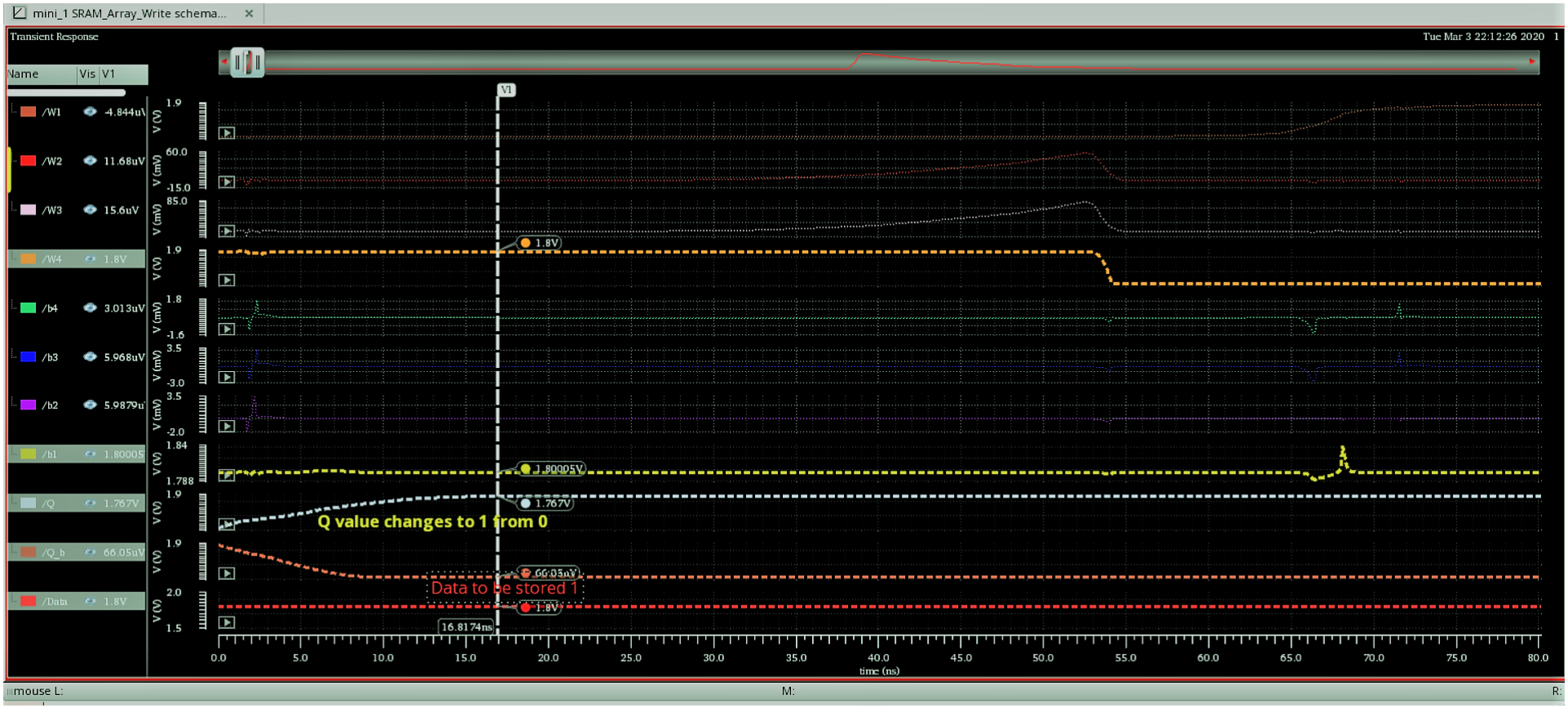
1. There are two 2X4 Decoders, 16 SRAM Cells, 8 Pass transistors in total for 4X4 SRAM Memory Cell.
2. Row Decoder is for selecting word lines of rows.
3. Each column Bit and Bit-bar ports are connected to a pair of pass transistors(with gates connected).
4. Output of the column decoder is connected to the gates of the Pass transistors.This type of configuration make sures that only one of the column is ON and others OFF.

Read Operation of 1 SRAM cell



1. Initially 1 is stored in SRAM cell of 4th row and 1st column. We need to read 1.(Row Decoder W4=1 & Column Decoder b1=1)
2. Initially both Data and Data-bar are precharged to high.
3. Here we can see that Data-bar decays to 0 and Data stays high, representing 1 is stored.

Write Operation of 1 SRAM cell



1. Initially 0 is stored in Q and 1 in Q-bar.
2. For writing we made Data as 1 and Data-bar as 0.
3. We can see that after selecting corresponding SRAM Cell(4 row ,1 column).1 is stored in Q and 0 in Q-bar.

5 main challenges/issues

Problem 1

- I faced a problem with column decoder and its connection with SRAM cells. It first involved a lot of NOT gates and AND gates to work.
- I solved this problem using a simple pass transistor logic. When one of the output of column decoder is 1, only one of the pass transistor is on (as NMOS turns on when input is high). So this way with minimal area and gates, we can do this.

Problem 2

- I faced a problem with assigned W/L values. The noise margin is not that great and delay is significant.
- With some other optimal W/L values, I got a good noise margin with minimal delay.

5 main challenges/issues

Problem 3

- During word bit transitioning from low to high, there should not be no action in SRAM cell until it is high. But the action of writing into SRAM cell starts in upper half of transition itself. Due to this, dynamic power dissipation happens and in practical, if there is a increase in word line to required value due to some reasons, write happens which is not desirable.

Problem 4

- Generally PMOS W/L should be minimum in SRAM for smooth functioning.
- But, in my design I tried with PMOS W/L keeping the highest among the all. The functioning of the circuit is fine because of the reason that mobility of holes is far less than mobility of electrons and my W/L values suited such that all functionalities work correct.

5 main challenges/issues

Problem 5

- The values that need to go to 0 are not reaching 0. There is a voltage in order of nV, wasting power.

Thank you